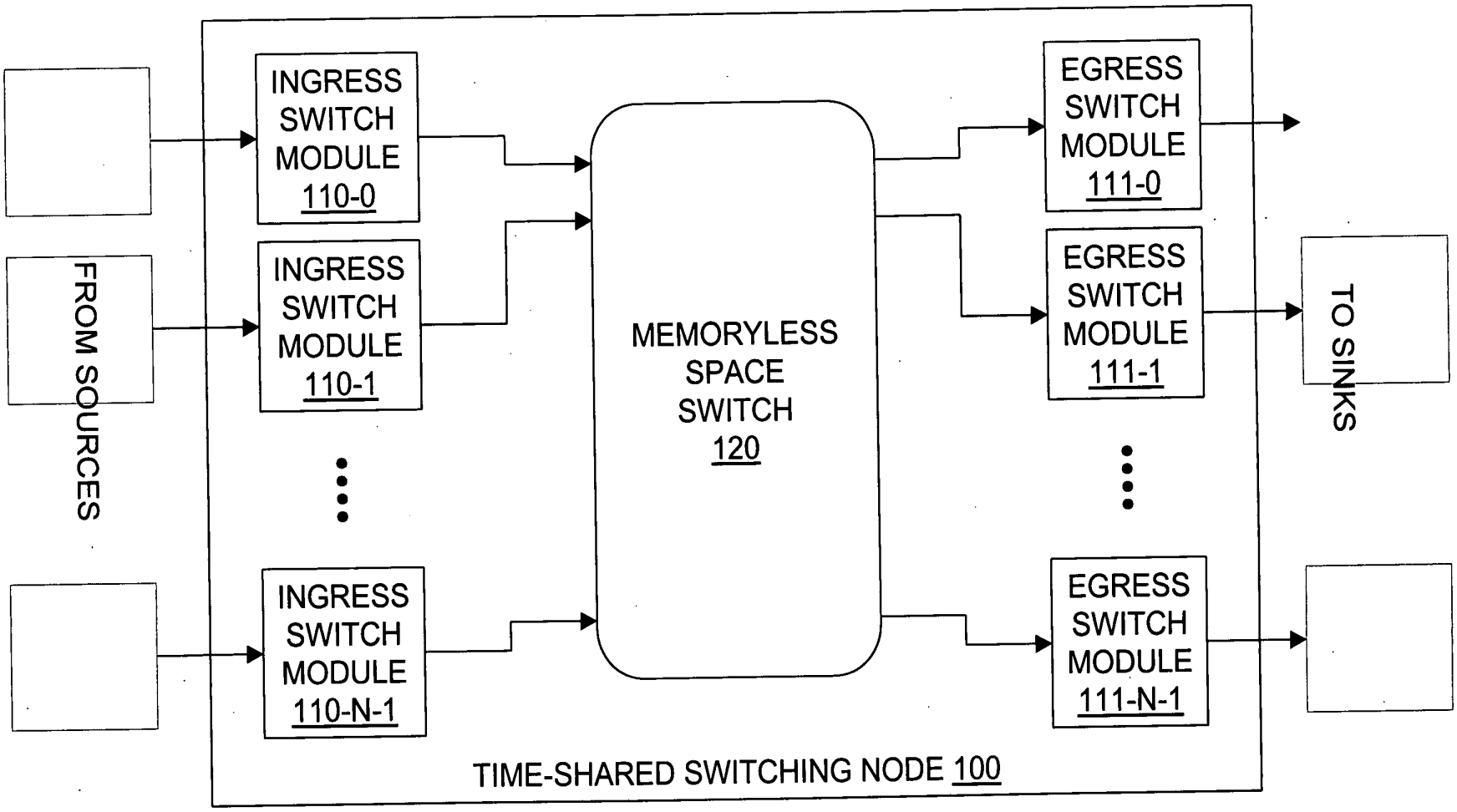
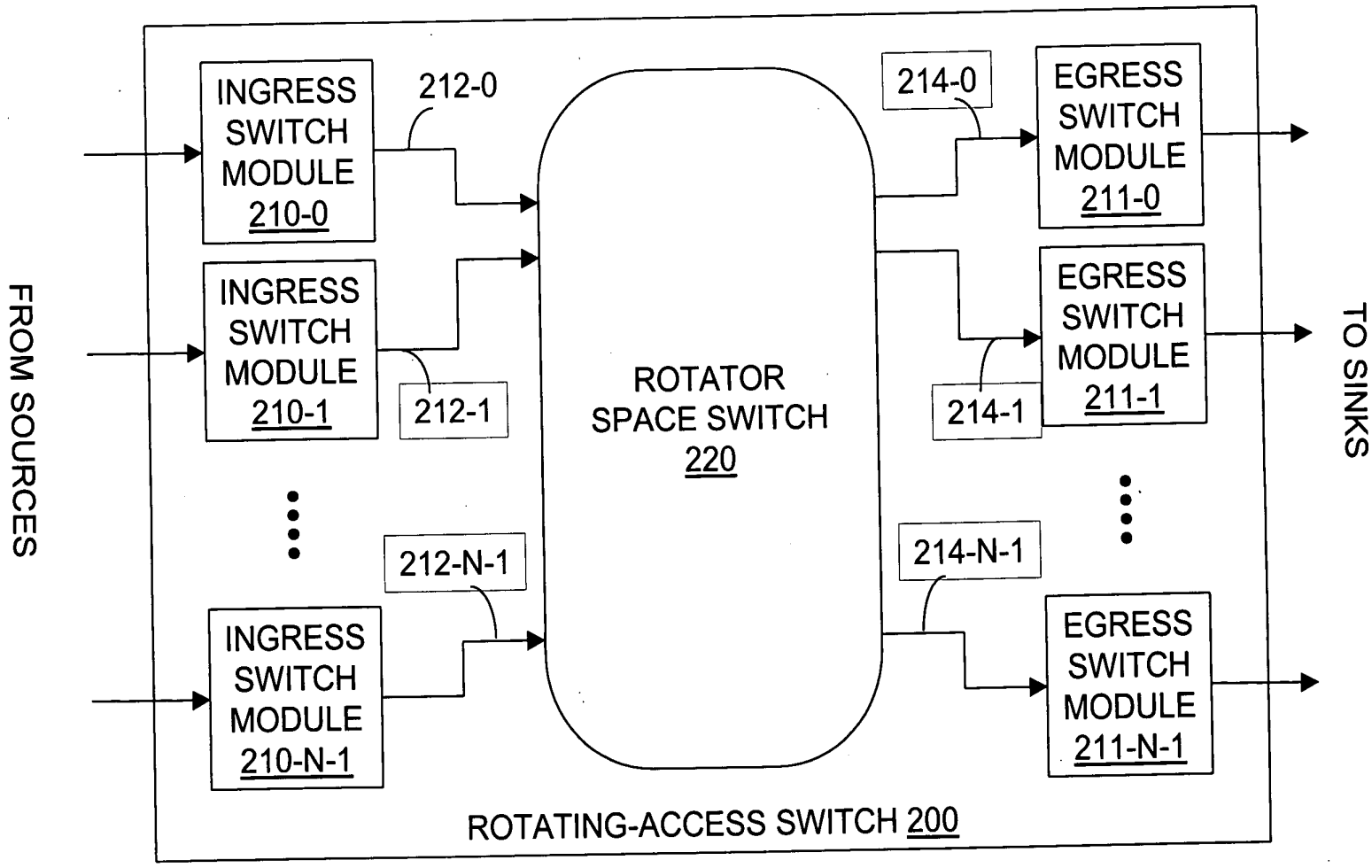


PRIOR ART

FIG. 1



PRIOR ART

FIG. 2

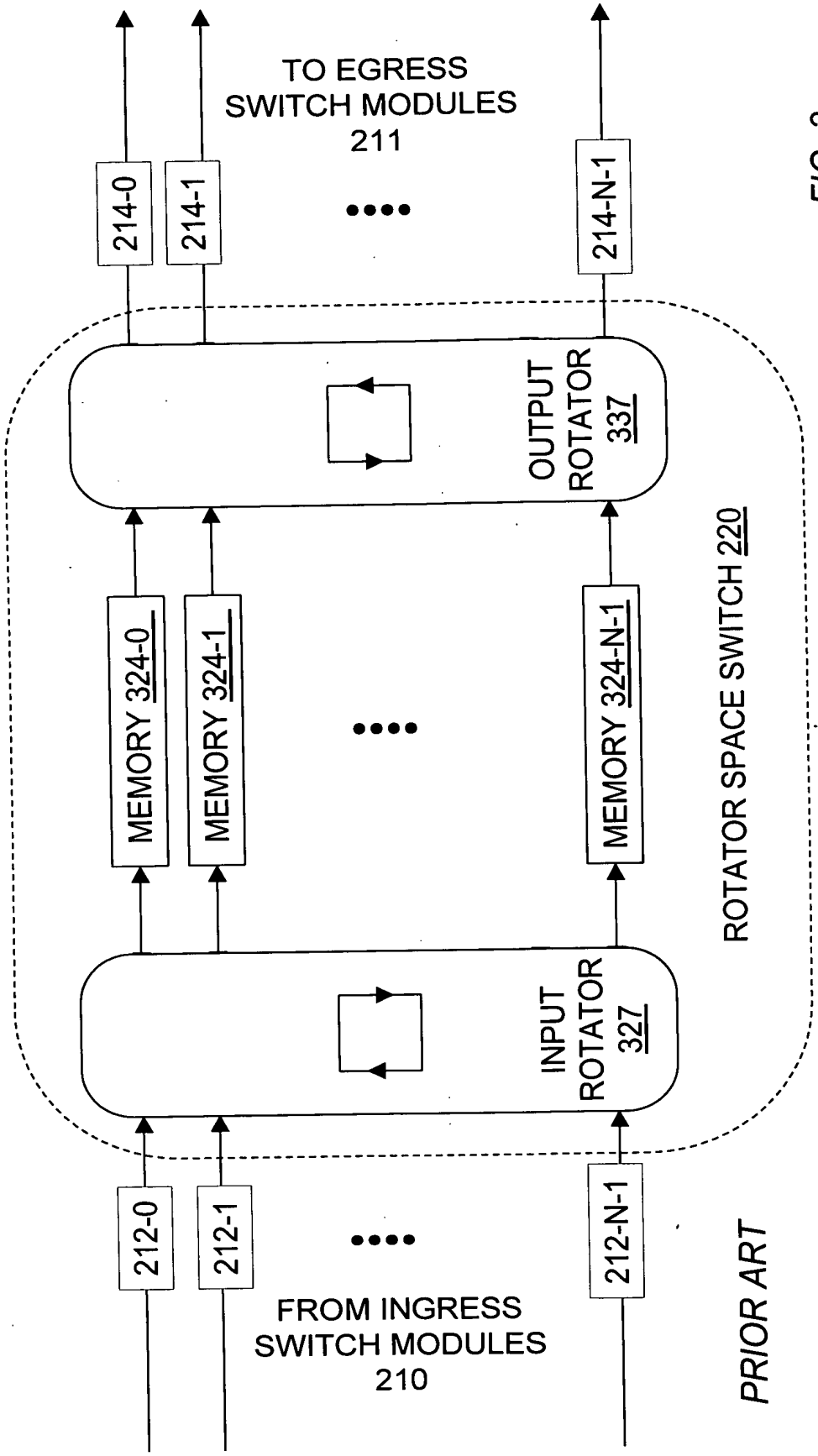

TO EGRESS SWITCH MODULES 211
214-0
214-1
214-N-1
OUTPUT ROTATOR 337
MEMORY 324-0
MEMORY 324-1
MEMORY 324-N-1
ROTATOR SPACE SWITCH 220
INPUT ROTATOR 327
212-0
212-1
212-N-1
FROM INGRESS SWITCH MODULES 210
PRIOR ART

FIG. 3

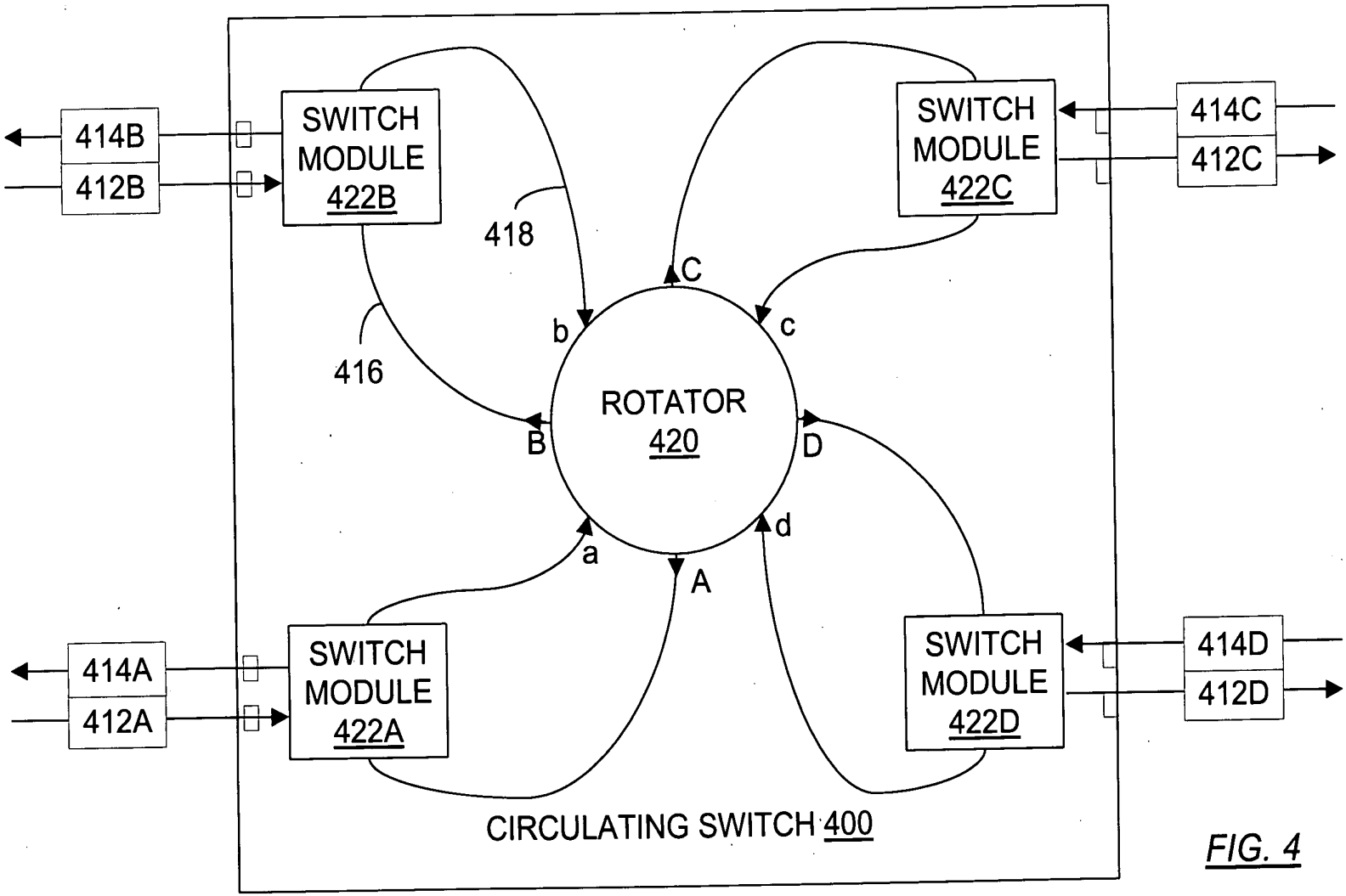

414B
412B
SWITCH MODULE 422B
418
416
b
C
c
SWITCH MODULE 422C
414C
412C
ROTATOR 420
B
D
a
A
d
414A
412A
SWITCH MODULE 422A
SWITCH MODULE 422D
414D
412D
CIRCULATING SWITCH 400

FIG. 4

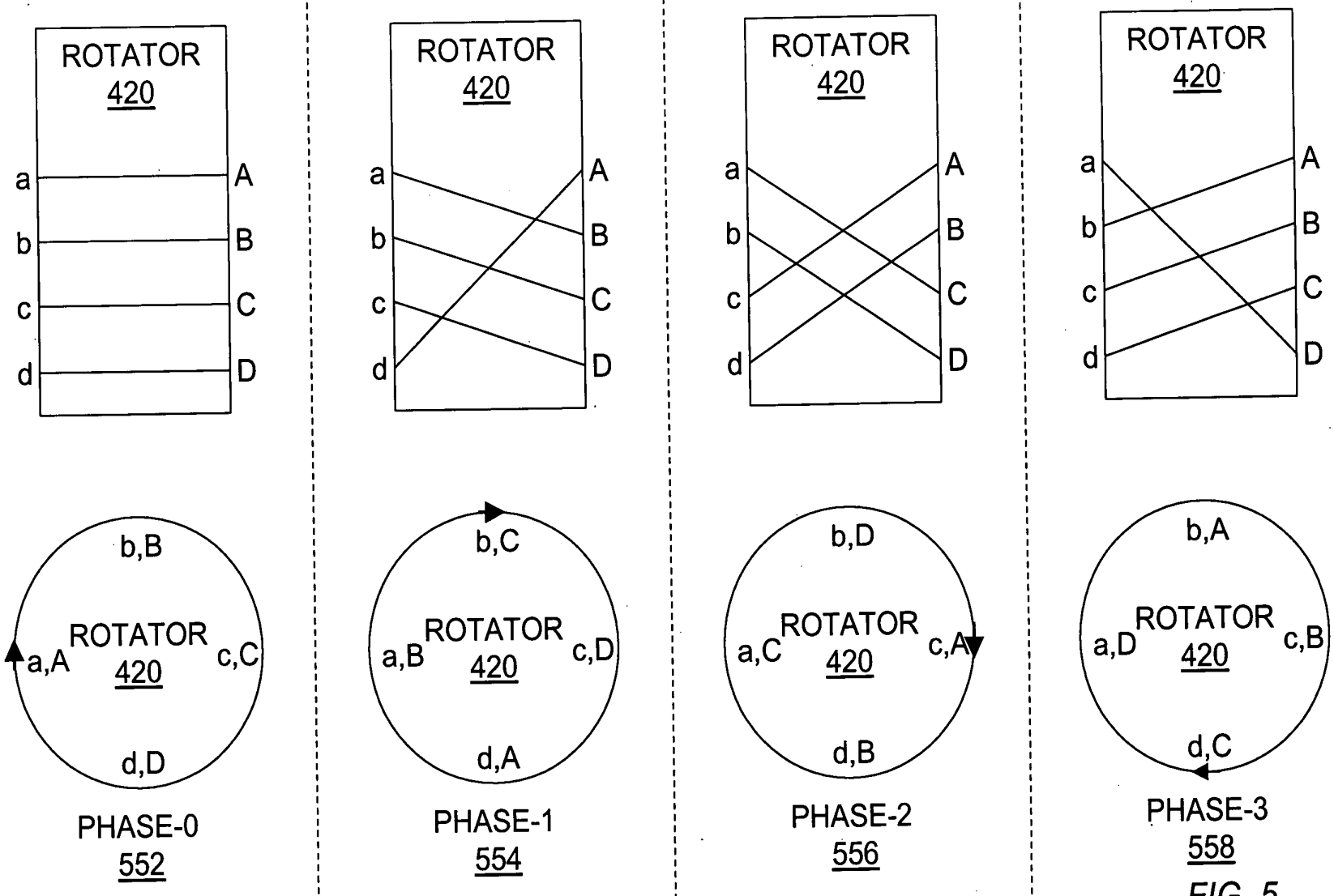

ROTATOR
420
a
b
c
d
A
B
C
D
b,B
a,A
c,C
d,D
PHASE-0
552
b,C
a,B
c,D
d,A
PHASE-1
554
b,D
a,C
c,A
d,B
PHASE-2
556
b,A
a,D
c,B
d,C
PHASE-3
558

FIG. 5

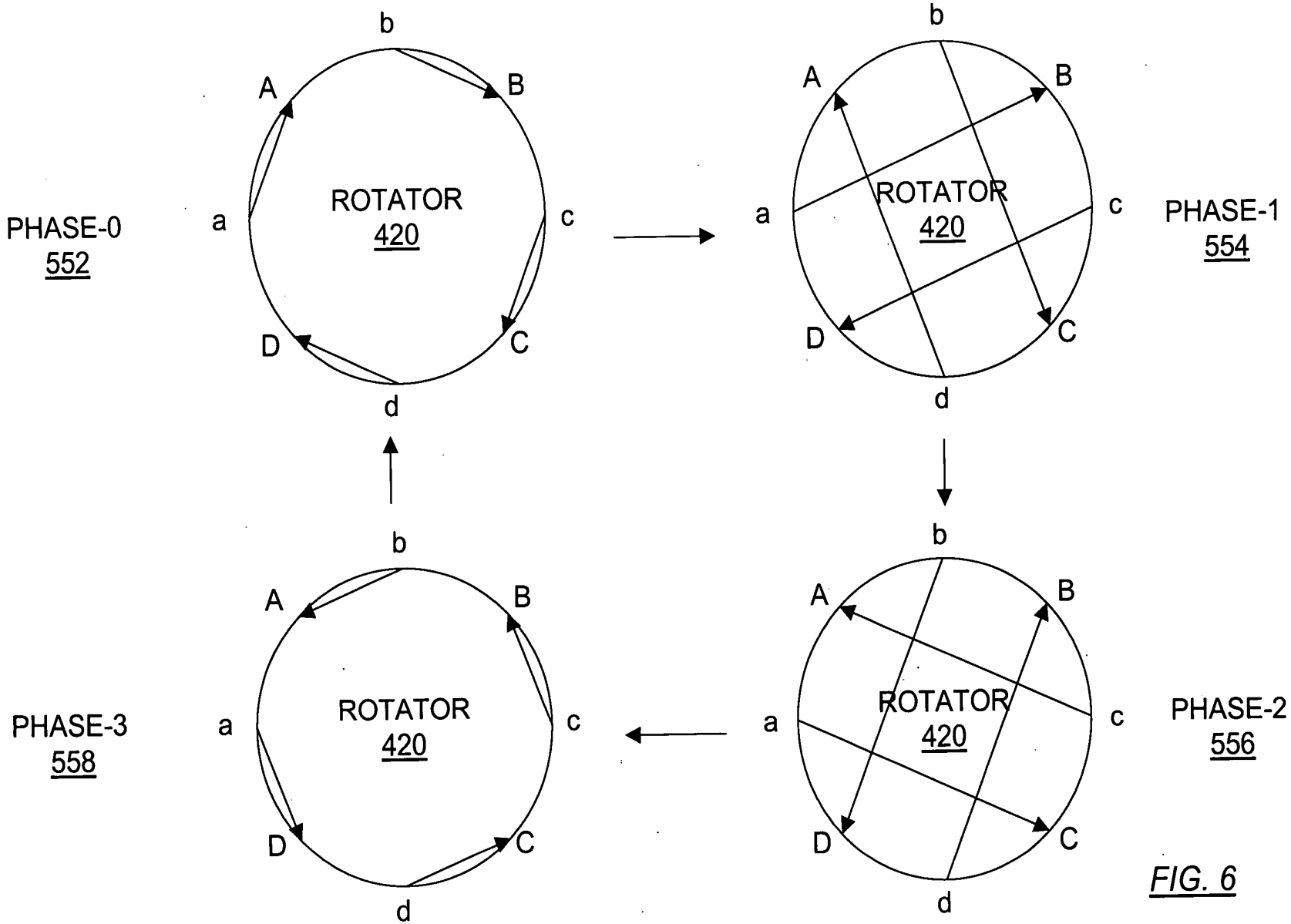

PHASE-0
552
ROTATOR
420
PHASE-1
554
PHASE-2
556
PHASE-3
558
A
B
C
D
a
b
c
d

FIG. 6

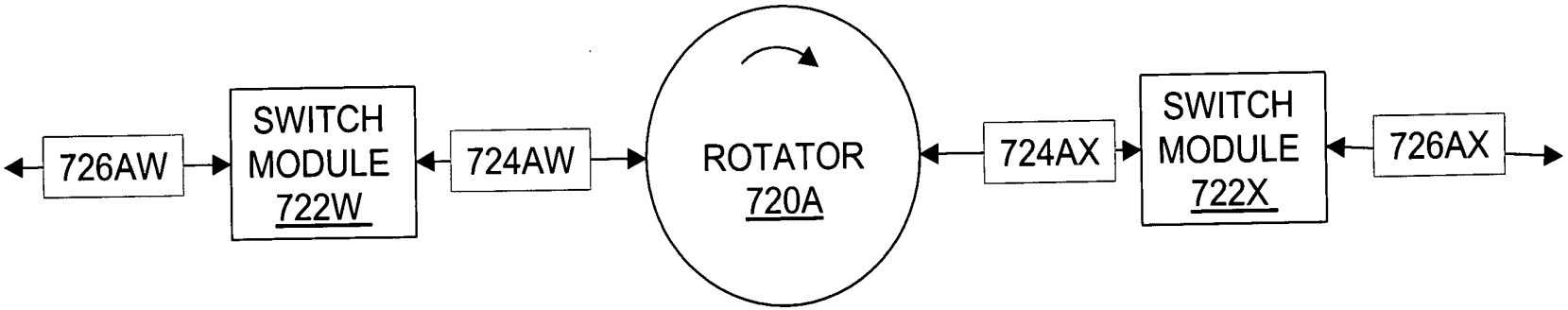

726AW
SWITCH MODULE 722W
724AW
ROTATOR 720A
724AX
SWITCH MODULE 722X
726AX

FIG. 7A

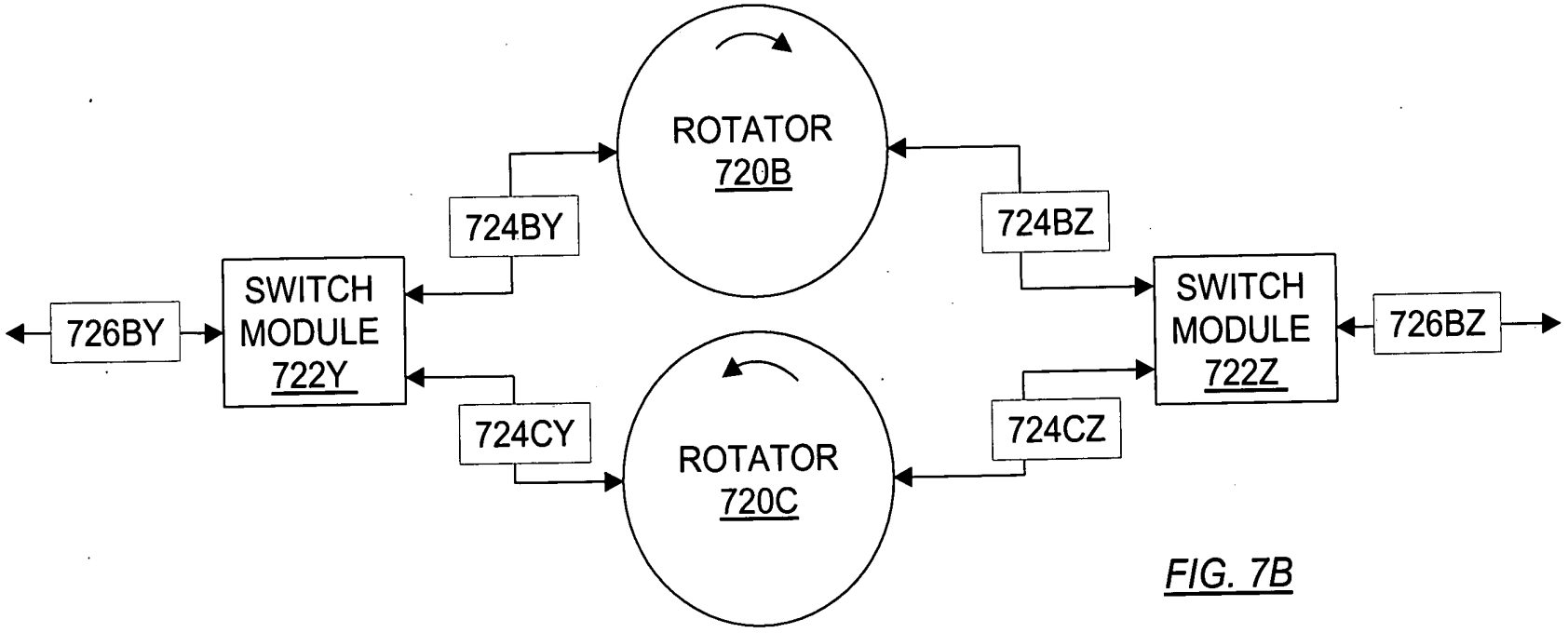

726BY
SWITCH MODULE 722Y
724BY
724CY
ROTATOR 720B
ROTATOR 720C
724BZ
724CZ
SWITCH MODULE 722Z
726BZ

FIG. 7B

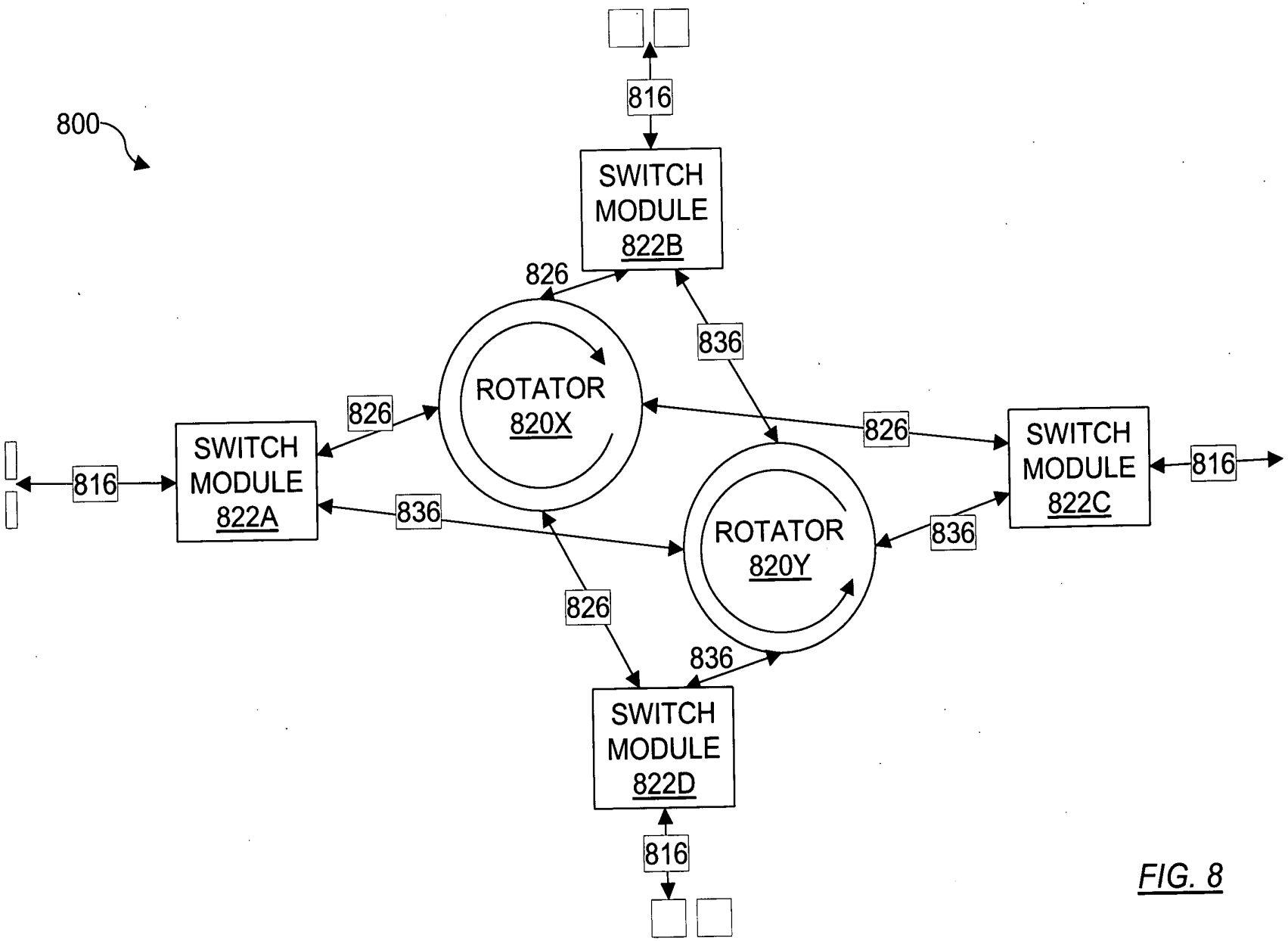

800
816
SWITCH MODULE 822B
826
836
ROTATOR 820X
826
826
SWITCH MODULE 822A
816
836
ROTATOR 820Y
836
SWITCH MODULE 822C
816
826
836
SWITCH MODULE 822D
816

FIG. 8

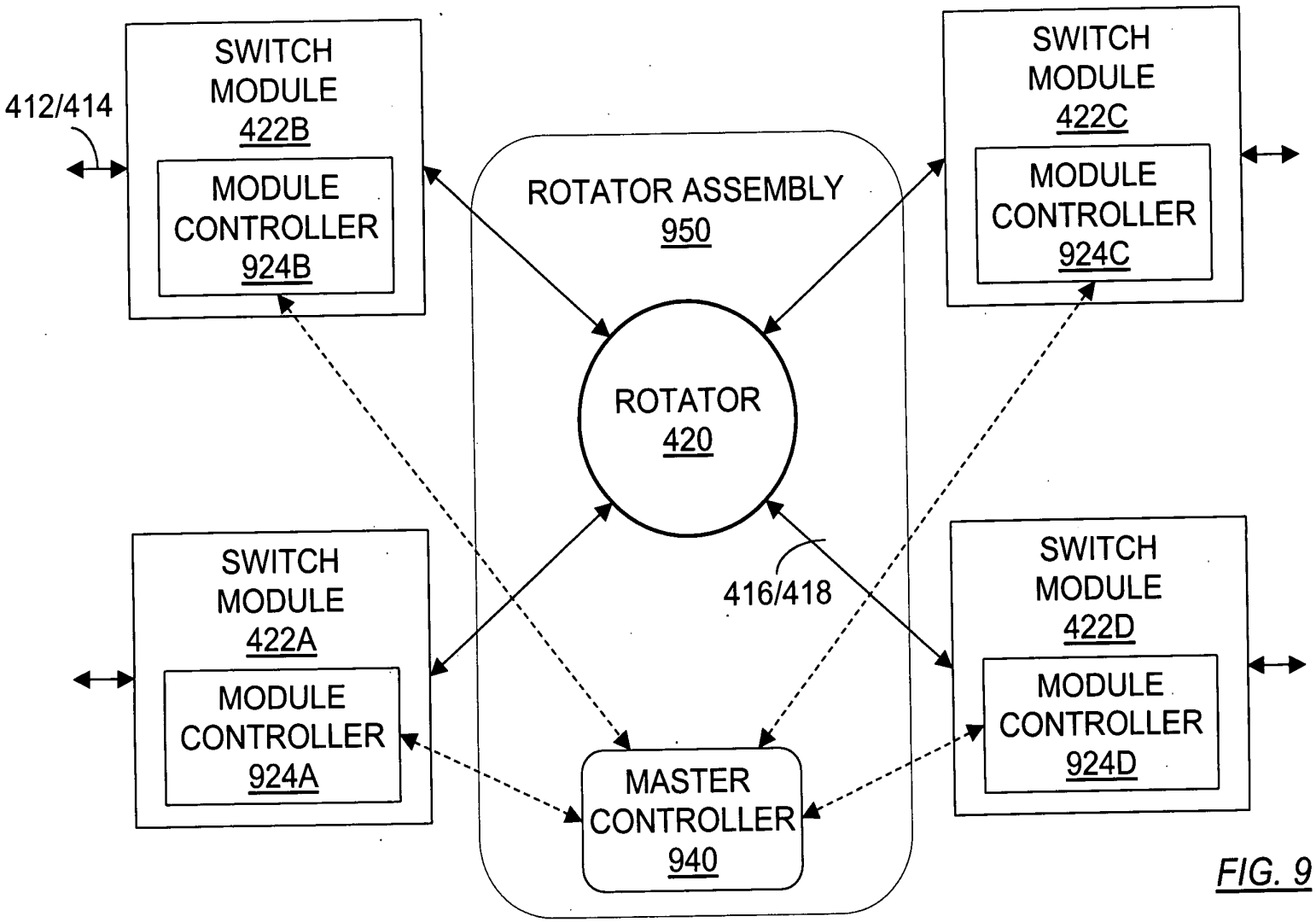

412/414
SWITCH MODULE 422B
MODULE CONTROLLER 924B
ROTATOR ASSEMBLY 950
ROTATOR 420
SWITCH MODULE 422C
MODULE CONTROLLER 924C
SWITCH MODULE 422A
MODULE CONTROLLER 924A
416/418
SWITCH MODULE 422D
MODULE CONTROLLER 924D
MASTER CONTROLLER 940

FIG. 9

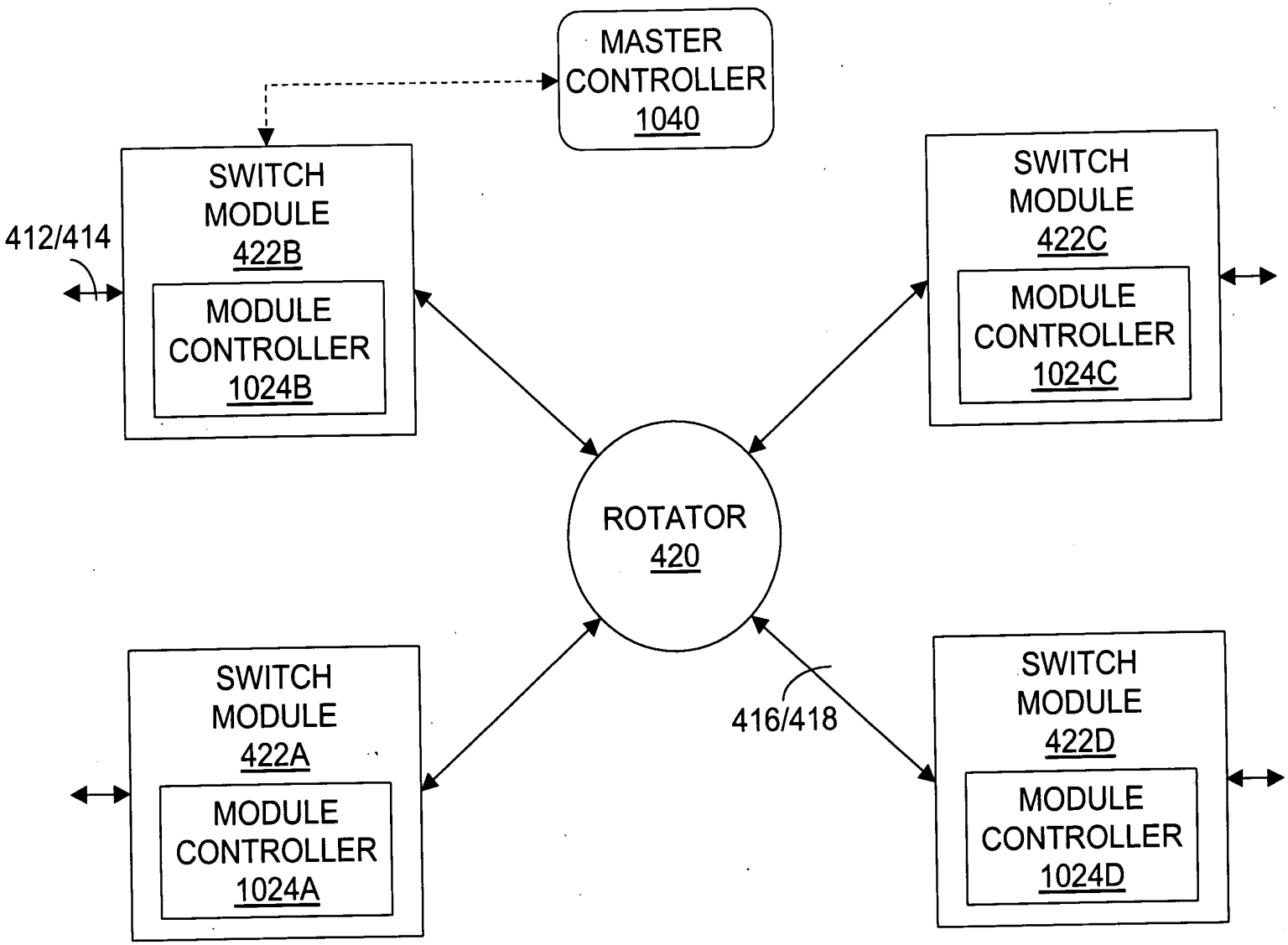

MASTER CONTROLLER 1040
SWITCH MODULE 422B
MODULE CONTROLLER 1024B
412/414
SWITCH MODULE 422C
MODULE CONTROLLER 1024C
ROTATOR 420
SWITCH MODULE 422A
MODULE CONTROLLER 1024A
416/418
SWITCH MODULE 422D
MODULE CONTROLLER 1024D

FIG. 10

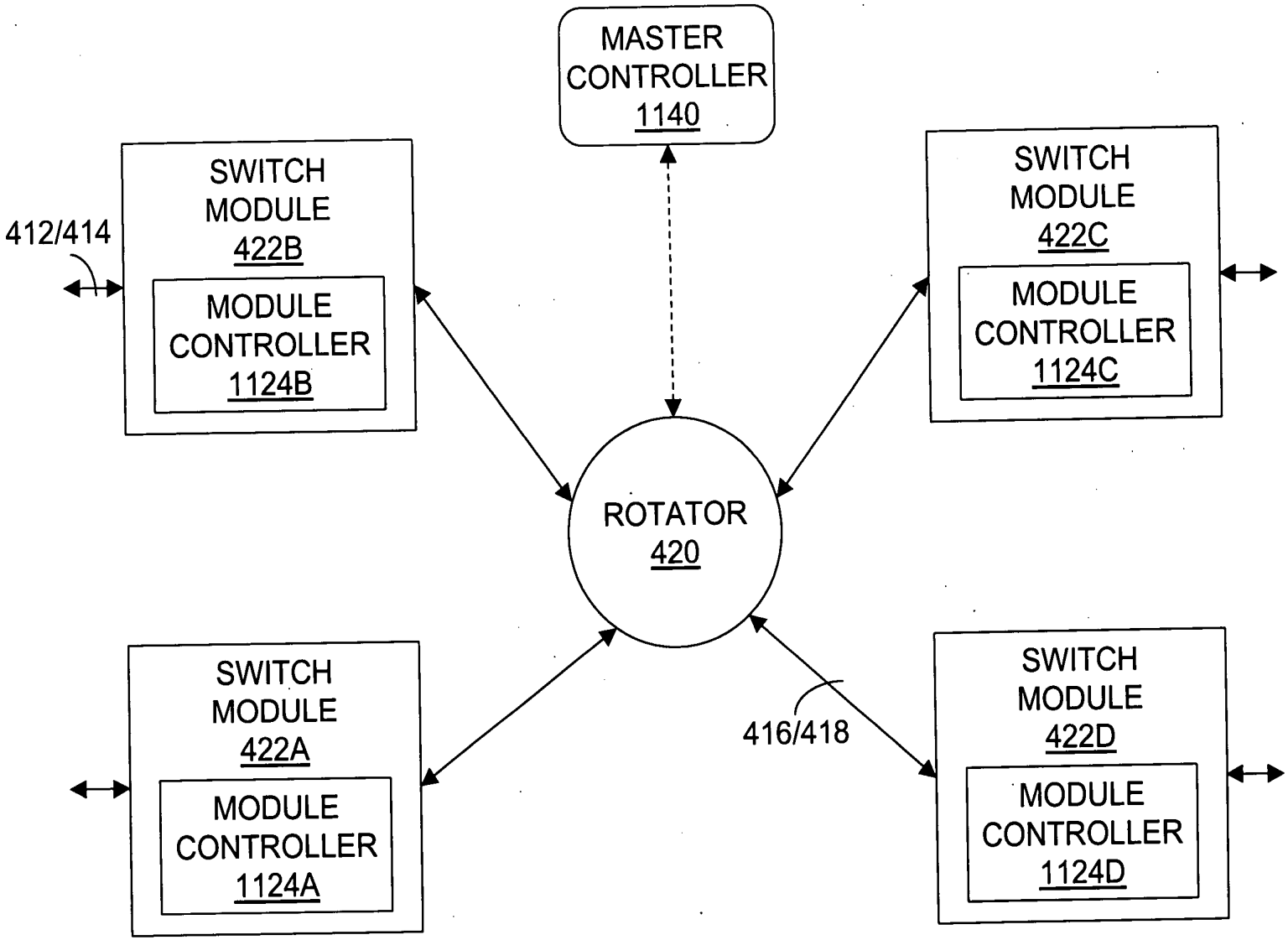

MASTER CONTROLLER 1140
SWITCH MODULE 422B
MODULE CONTROLLER 1124B
412/414
SWITCH MODULE 422C
MODULE CONTROLLER 1124C
ROTATOR 420
SWITCH MODULE 422A
MODULE CONTROLLER 1124A
416/418
SWITCH MODULE 422D
MODULE CONTROLLER 1124D

FIG. 11

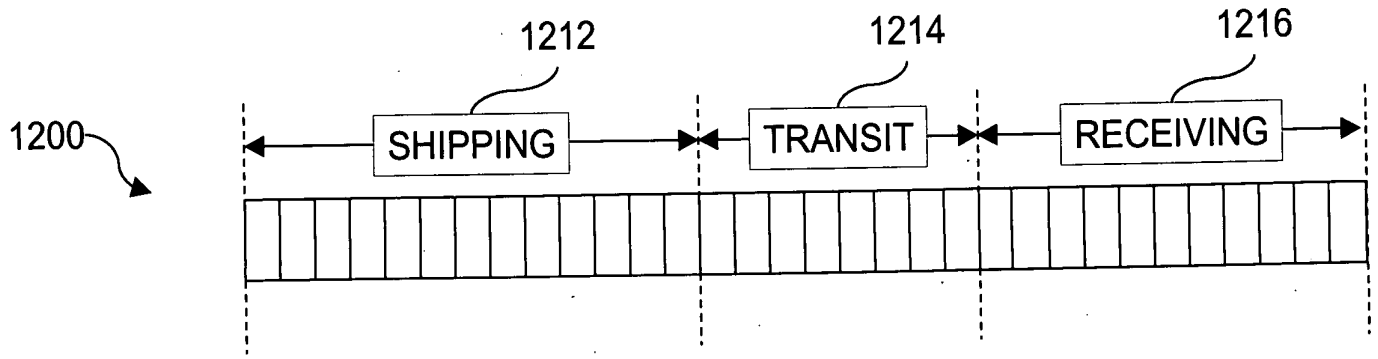


FIG. 12

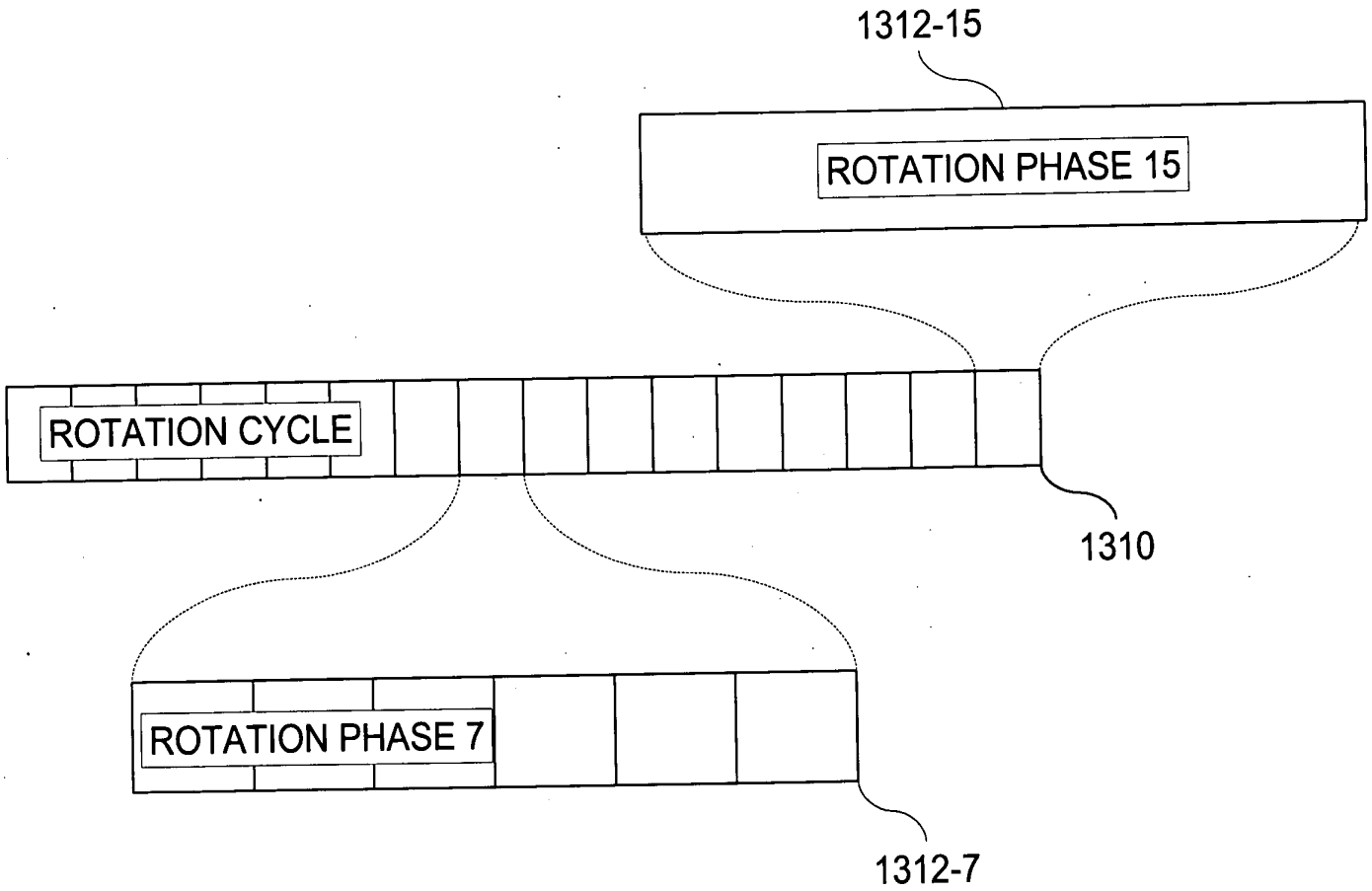

1312-15
ROTATION PHASE 15
ROTATION CYCLE
1310
ROTATION PHASE 7
1312-7

FIG. 13

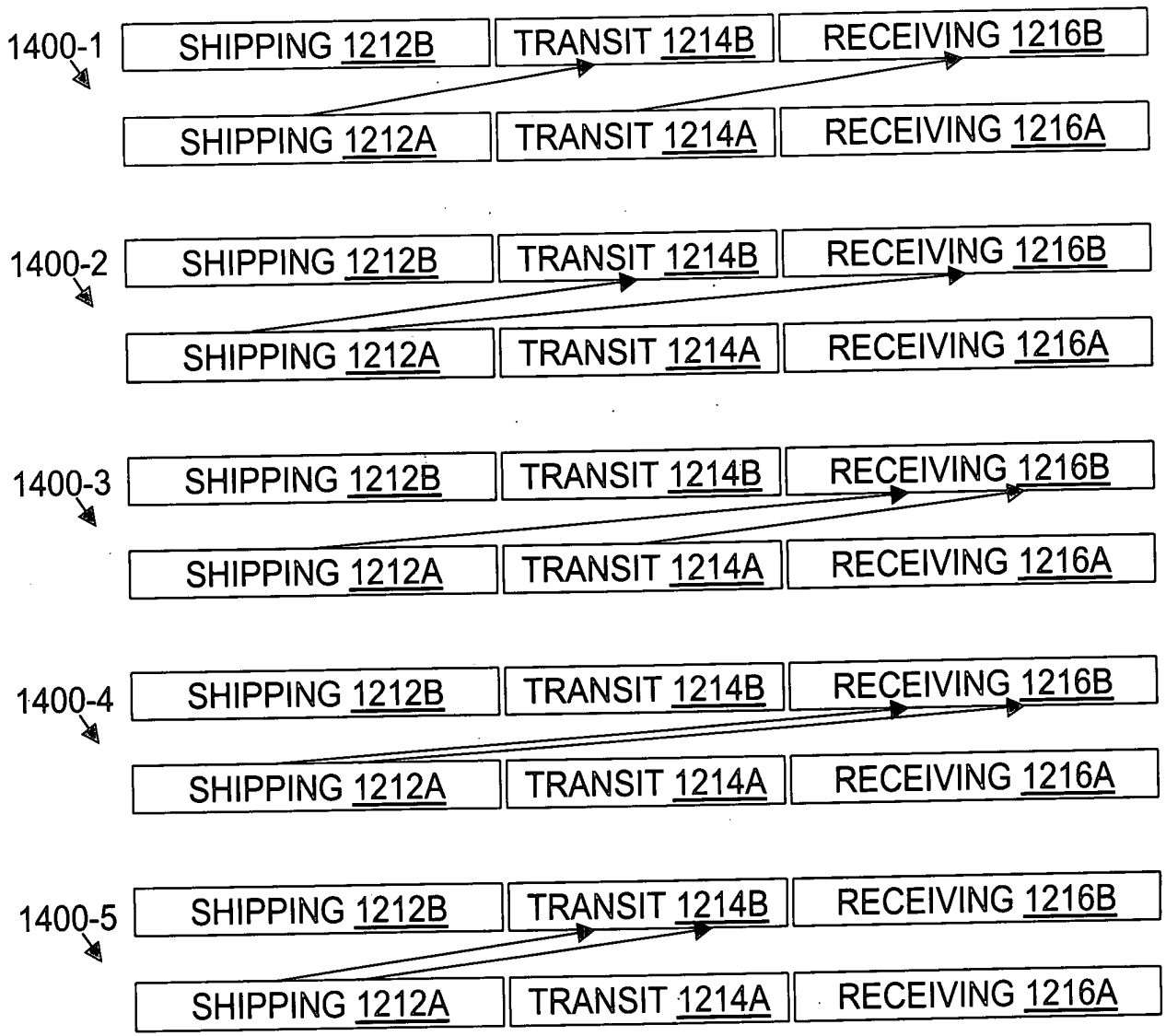

1400-1
SHIPPING 1212B
TRANSIT 1214B
RECEIVING 1216B
SHIPPING 1212A
TRANSIT 1214A
RECEIVING 1216A
1400-2
SHIPPING 1212B
TRANSIT 1214B
RECEIVING 1216B
SHIPPING 1212A
TRANSIT 1214A
RECEIVING 1216A
1400-3
SHIPPING 1212B
TRANSIT 1214B
RECEIVING 1216B
SHIPPING 1212A
TRANSIT 1214A
RECEIVING 1216A
1400-4
SHIPPING 1212B
TRANSIT 1214B
RECEIVING 1216B
SHIPPING 1212A
TRANSIT 1214A
RECEIVING 1216A
1400-5
SHIPPING 1212B
TRANSIT 1214B
RECEIVING 1216B
SHIPPING 1212A
TRANSIT 1214A
RECEIVING 1216A

FIG. 14

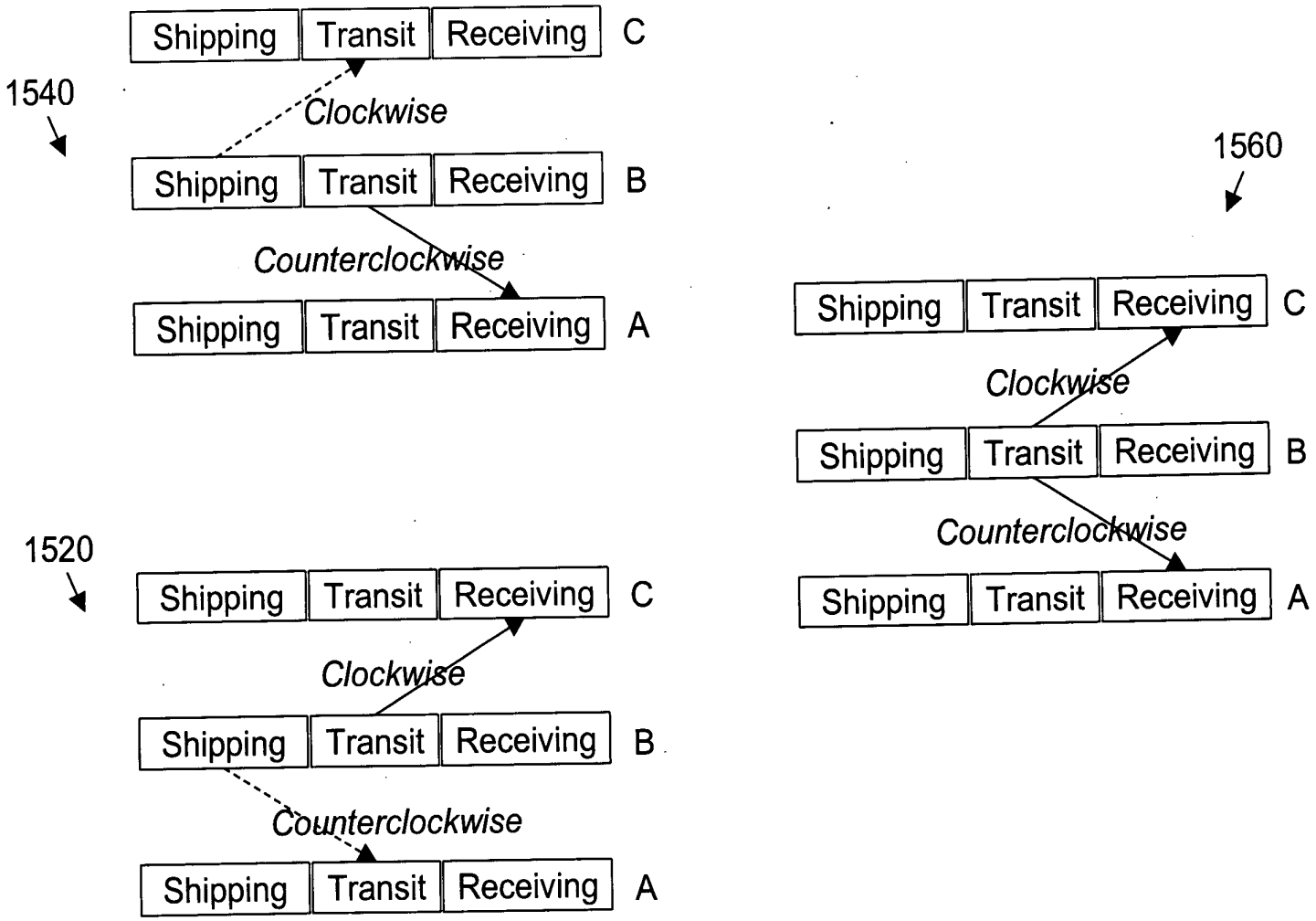

1540
Shipping
Transit
Receiving
C
Clockwise
Shipping
Transit
Receiving
B
Counterclockwise
Shipping
Transit
Receiving
A
1560
Shipping
Transit
Receiving
C
Clockwise
Shipping
Transit
Receiving
B
Counterclockwise
Shipping
Transit
Receiving
A
1520
Shipping
Transit
Receiving
C
Clockwise
Shipping
Transit
Receiving
B
Counterclockwise
Shipping
Transit
Receiving
A

FIG. 15

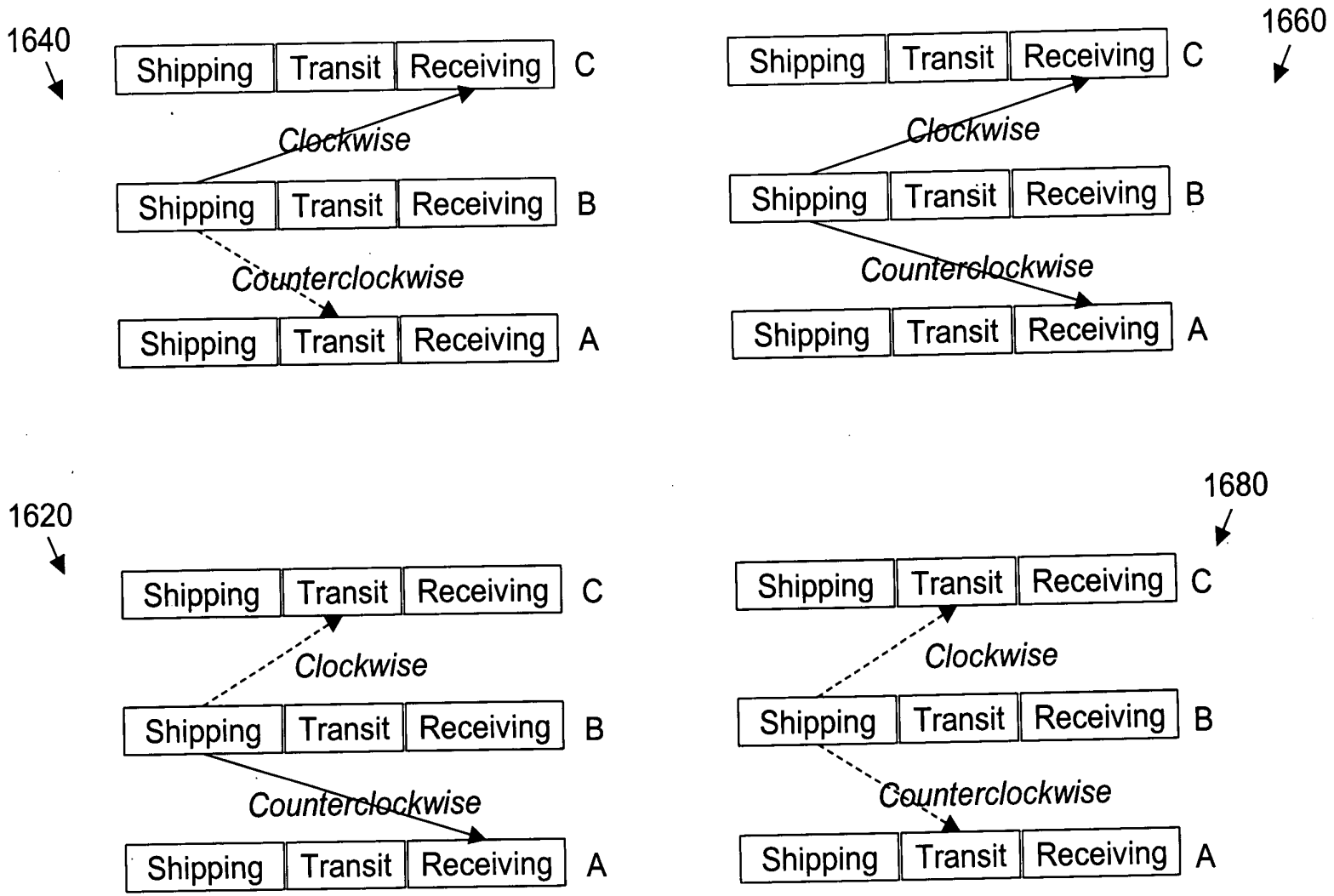

1640
Shipping
Transit
Receiving
C
Clockwise
Shipping
Transit
Receiving
B
Counterclockwise
Shipping
Transit
Receiving
A
1660
Shipping
Transit
Receiving
C
Clockwise
Shipping
Transit
Receiving
B
Counterclockwise
Shipping
Transit
Receiving
A
1620
Shipping
Transit
Receiving
C
Clockwise
Shipping
Transit
Receiving
B
Counterclockwise
Shipping
Transit
Receiving
A
1680
Shipping
Transit
Receiving
C
Clockwise
Shipping
Transit
Receiving
B
Counterclockwise
Shipping
Transit
Receiving
A

FIG. 16

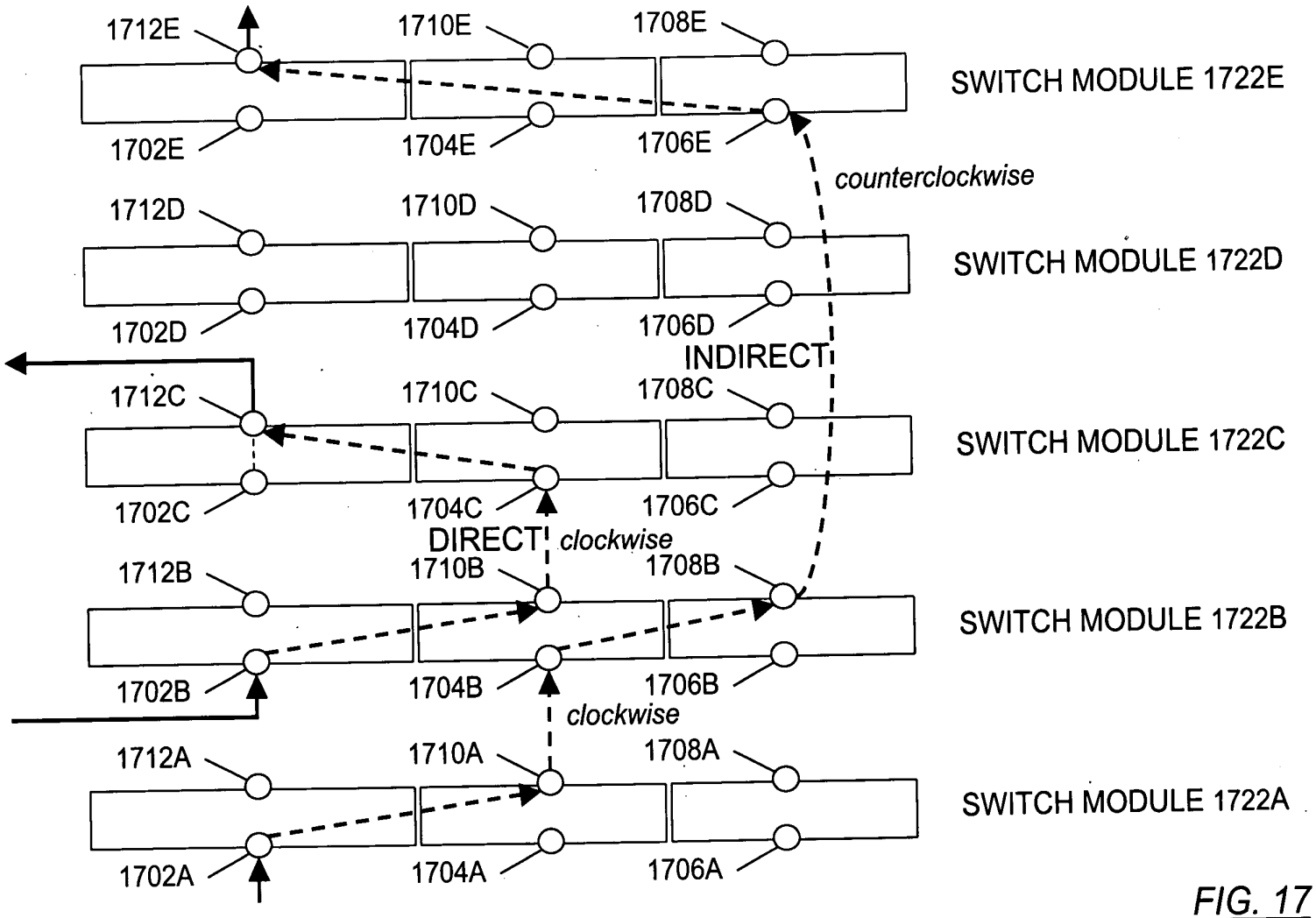

1712E
1710E
1708E
SWITCH MODULE 1722E
1702E
1704E
1706E
counterclockwise
1712D
1710D
1708D
SWITCH MODULE 1722D
1702D
1704D
1706D
INDIRECT
1712C
1710C
1708C
SWITCH MODULE 1722C
1702C
1704C
1706C
DIRECT
clockwise
1712B
1710B
1708B
SWITCH MODULE 1722B
1702B
1704B
1706B
clockwise
1712A
1710A
1708A
SWITCH MODULE 1722A
1702A
1704A
1706A

FIG. 17

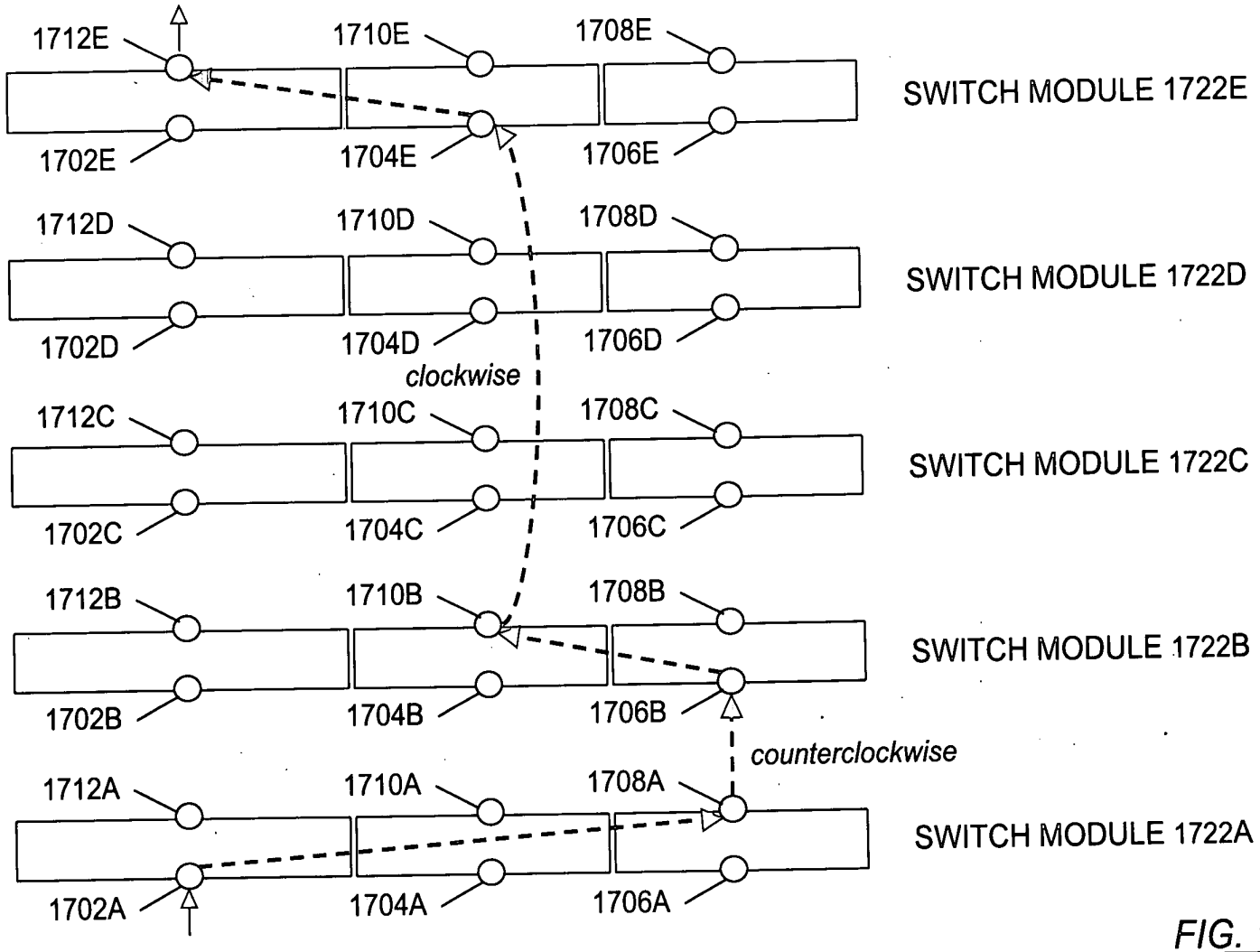

1712E
1710E
1708E
SWITCH MODULE 1722E
1702E
1704E
1706E
1712D
1710D
1708D
SWITCH MODULE 1722D
1702D
1704D
1706D
clockwise
1712C
1710C
1708C
SWITCH MODULE 1722C
1702C
1704C
1706C
1712B
1710B
1708B
SWITCH MODULE 1722B
1702B
1704B
1706B
counterclockwise
1712A
1710A
1708A
SWITCH MODULE 1722A
1702A
1704A
1706A

FIG. 18

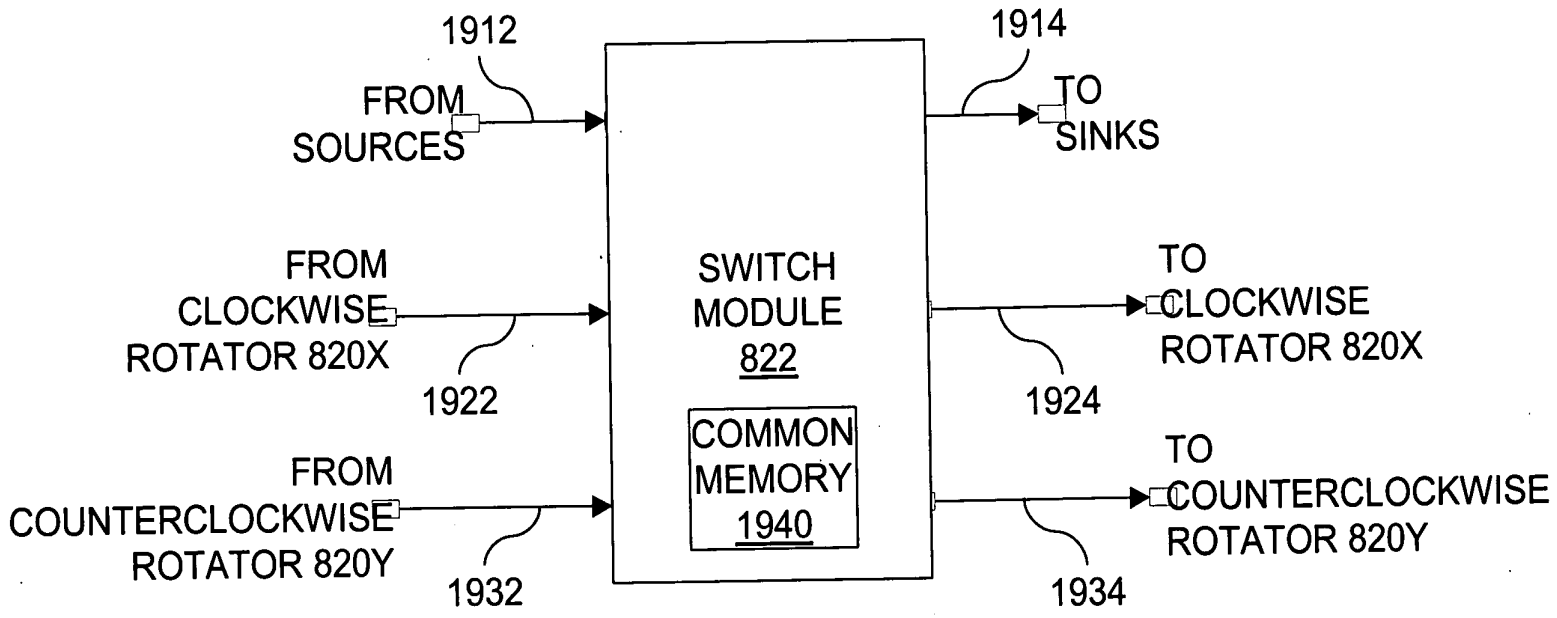

1912
FROM
SOURCES
1914
TO
SINKS
FROM
CLOCKWISE
ROTATOR 820X
1922
SWITCH
MODULE
822
COMMON
MEMORY
1940
TO
CLOCKWISE
ROTATOR 820X
1924
FROM
COUNTERCLOCKWISE
ROTATOR 820Y
1932
TO
COUNTERCLOCKWISE
ROTATOR 820Y
1934

FIG. 19

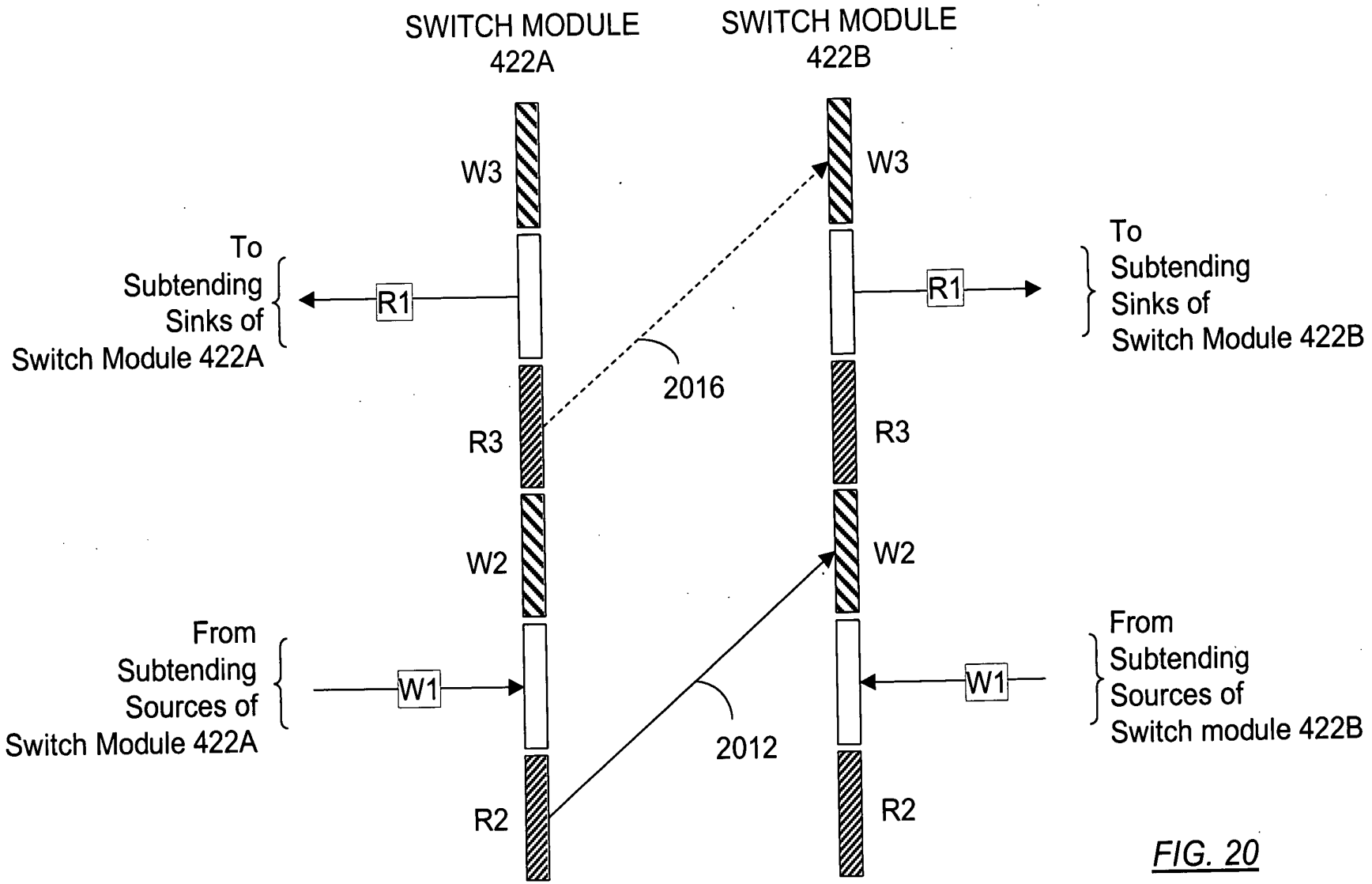

SWITCH MODULE
422A
SWITCH MODULE
422B
W3
W3
To
Subtending
Sinks of
Switch Module 422A
R1
R1
To
Subtending
Sinks of
Switch Module 422B
2016
R3
R3
W2
W2
From
Subtending
Sources of
Switch Module 422A
W1
W1
From
Subtending
Sources of
Switch module 422B
2012
R2
R2

FIG. 20

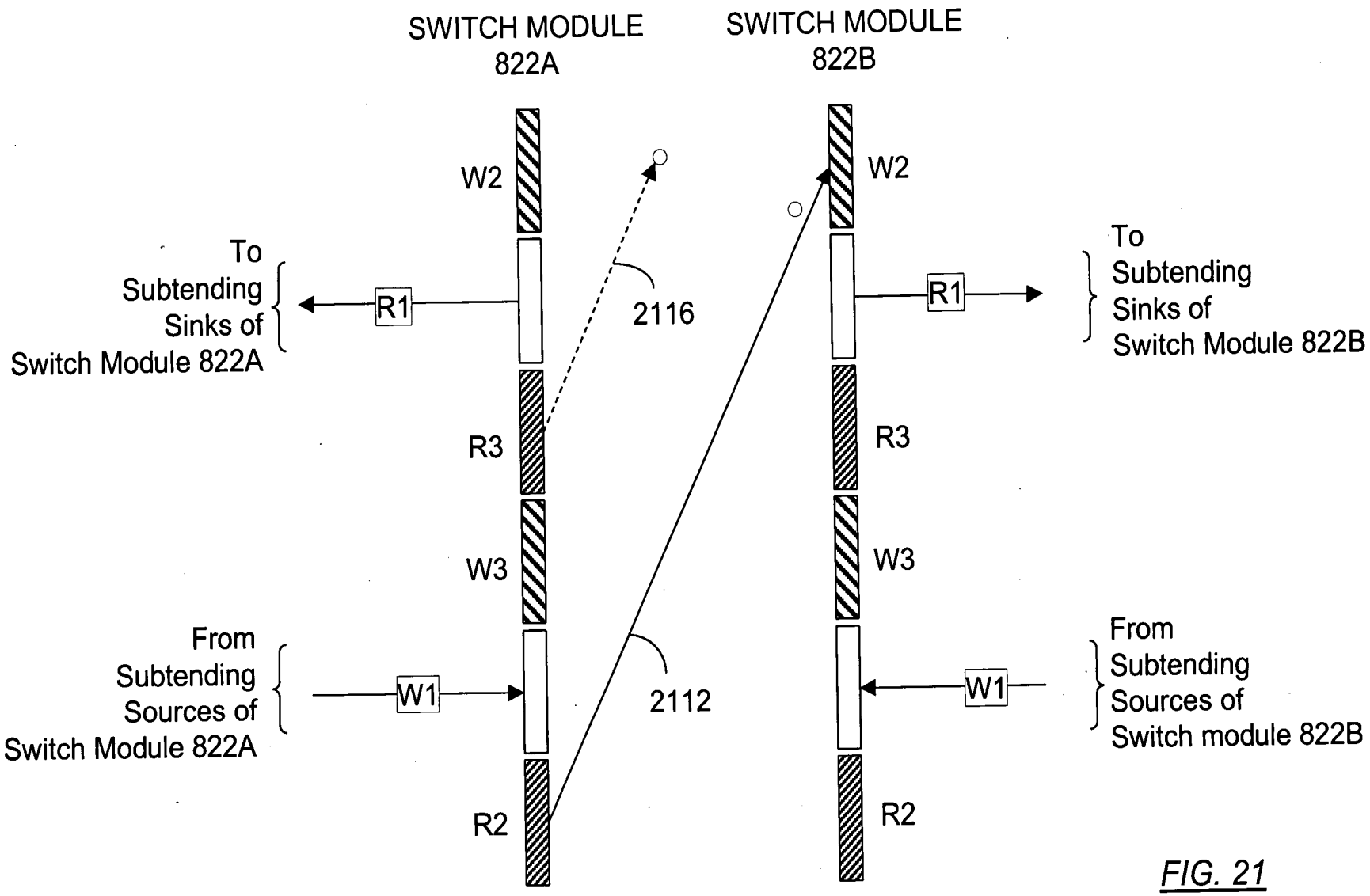
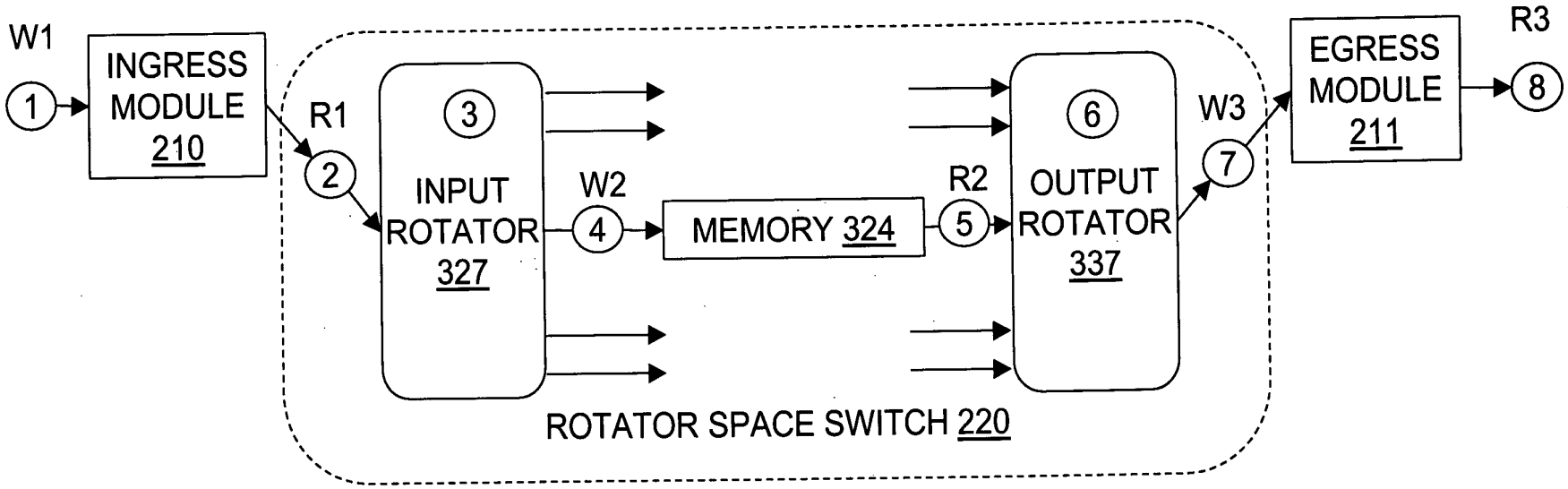

SWITCH MODULE
822A
SWITCH MODULE
822B
W2
W2
To
Subtending
Sinks of
Switch Module 822A
R1
2116
R1
To
Subtending
Sinks of
Switch Module 822B
R3
R3
W3
W3
From
Subtending
Sources of
Switch Module 822A
W1
2112
W1
From
Subtending
Sources of
Switch module 822B
R2
R2

FIG. 21



PRIOR ART

FIG. 22

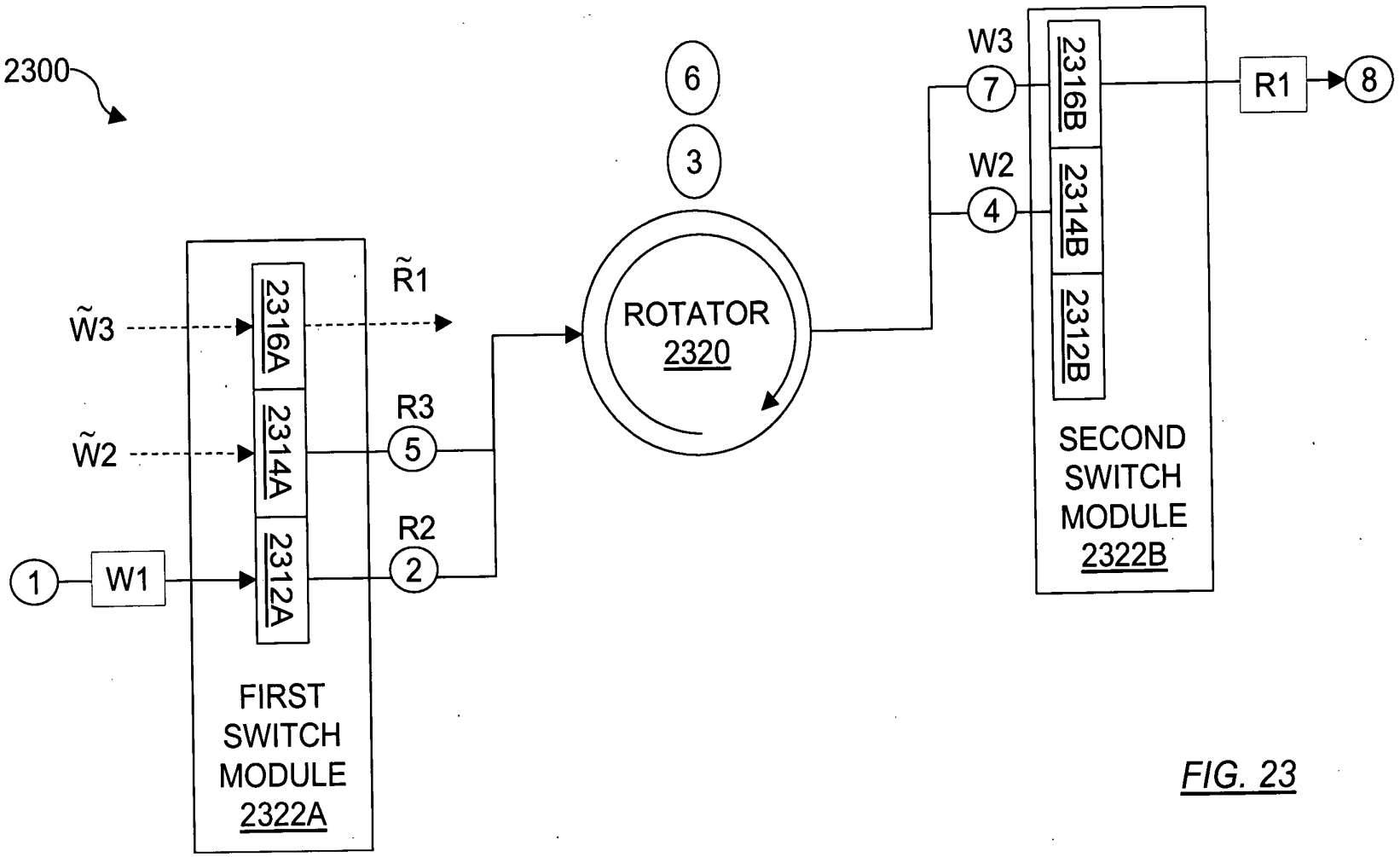

2300
6
3
W3
7
W2
4
2316B
2314B
2312B
R1
8
SECOND SWITCH MODULE 2322B
ROTATOR 2320
$\tilde{W}3$
$\tilde{W}2$
1
W1
2316A
2314A
2312A
$\tilde{R}1$
R3
5
R2
2
FIRST SWITCH MODULE 2322A

FIG. 23

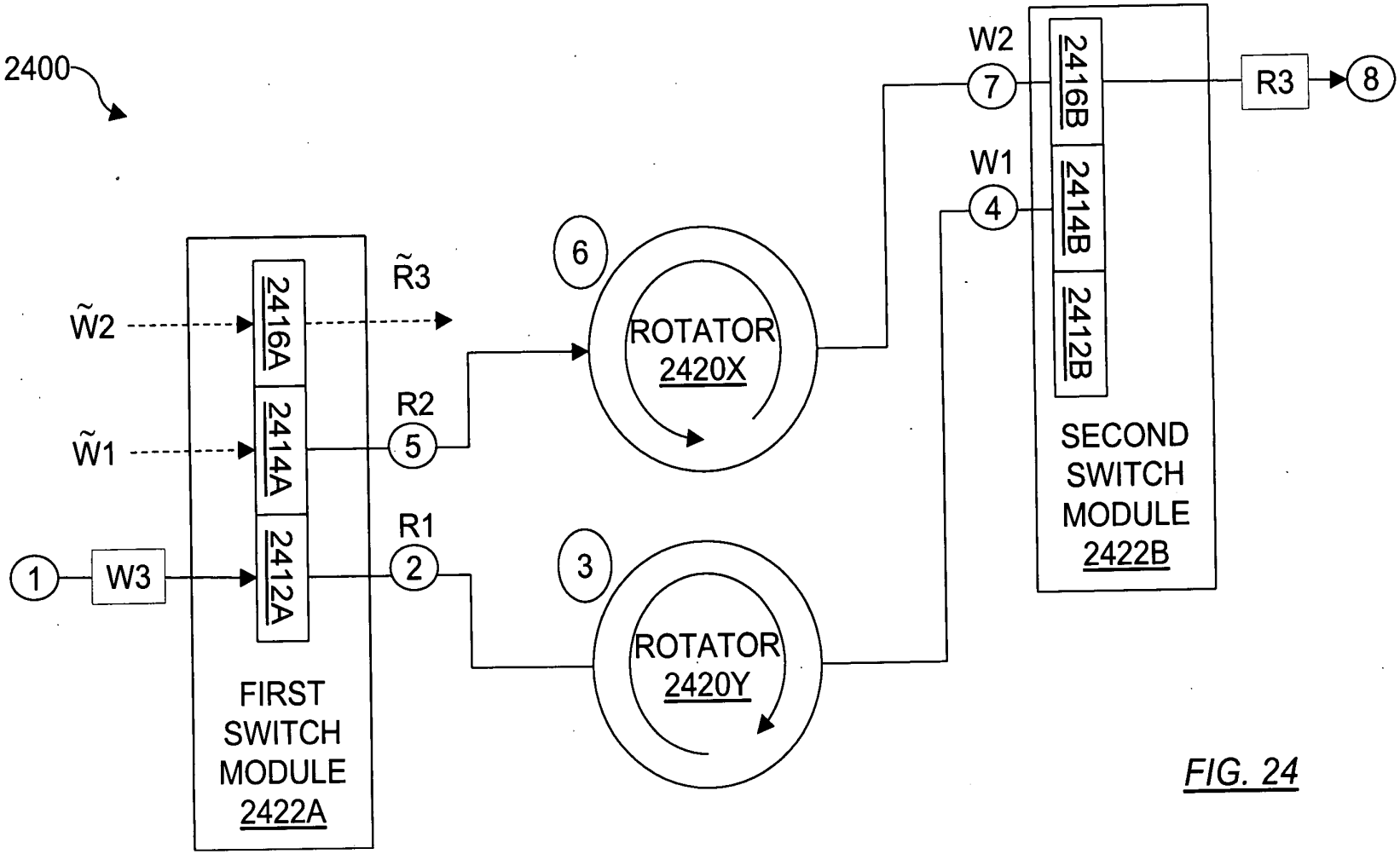

2400
W2
7
2416B
R3
8
W1
4
2414B
2412B
SECOND SWITCH MODULE 2422B
6
ROTATOR 2420X
R3
W2
2416A
2414A
2412A
R2
5
W1
R1
2
1
W3
3
ROTATOR 2420Y
FIRST SWITCH MODULE 2422A

FIG. 24

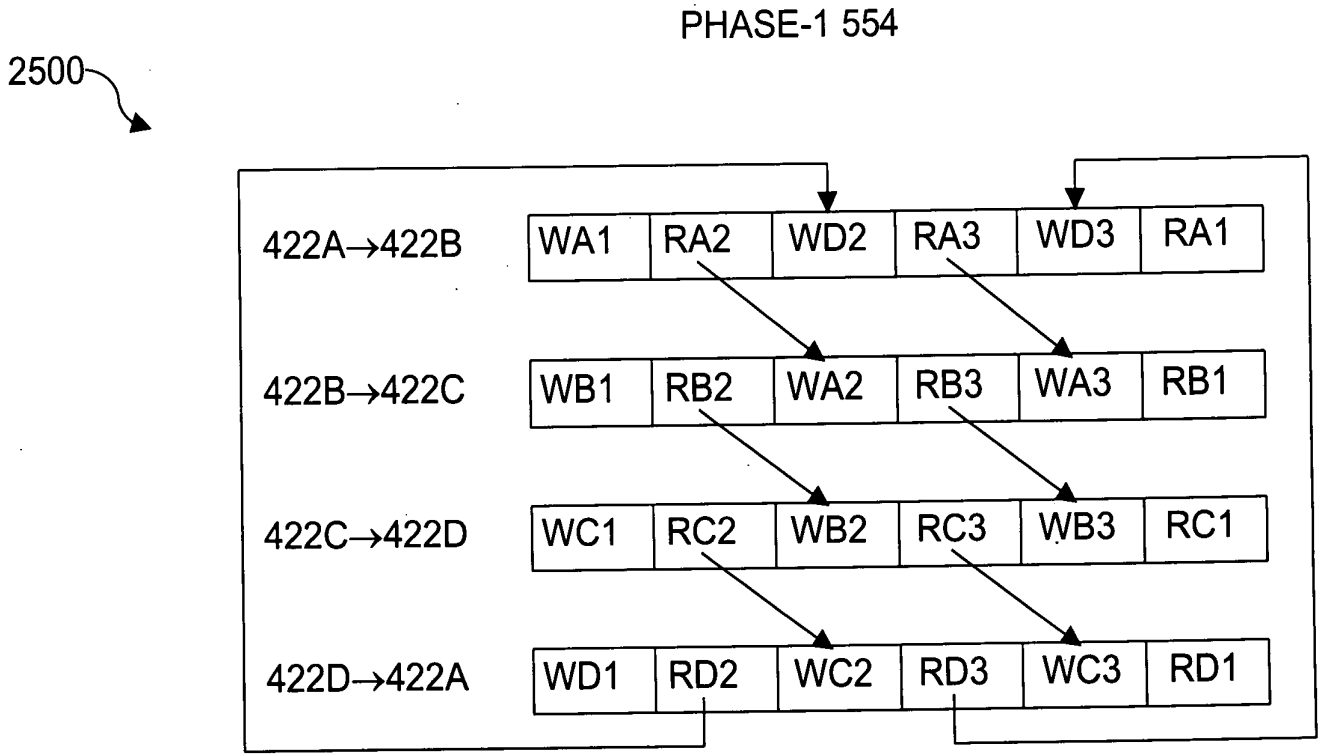

PHASE-1 554
2500
422A→422B
WA1
RA2
WD2
RA3
WD3
RA1
422B→422C
WB1
RB2
WA2
RB3
WA3
RB1
422C→422D
WC1
RC2
WB2
RC3
WB3
RC1
422D→422A
WD1
RD2
WC2
RD3
WC3
RD1

FIG. 25

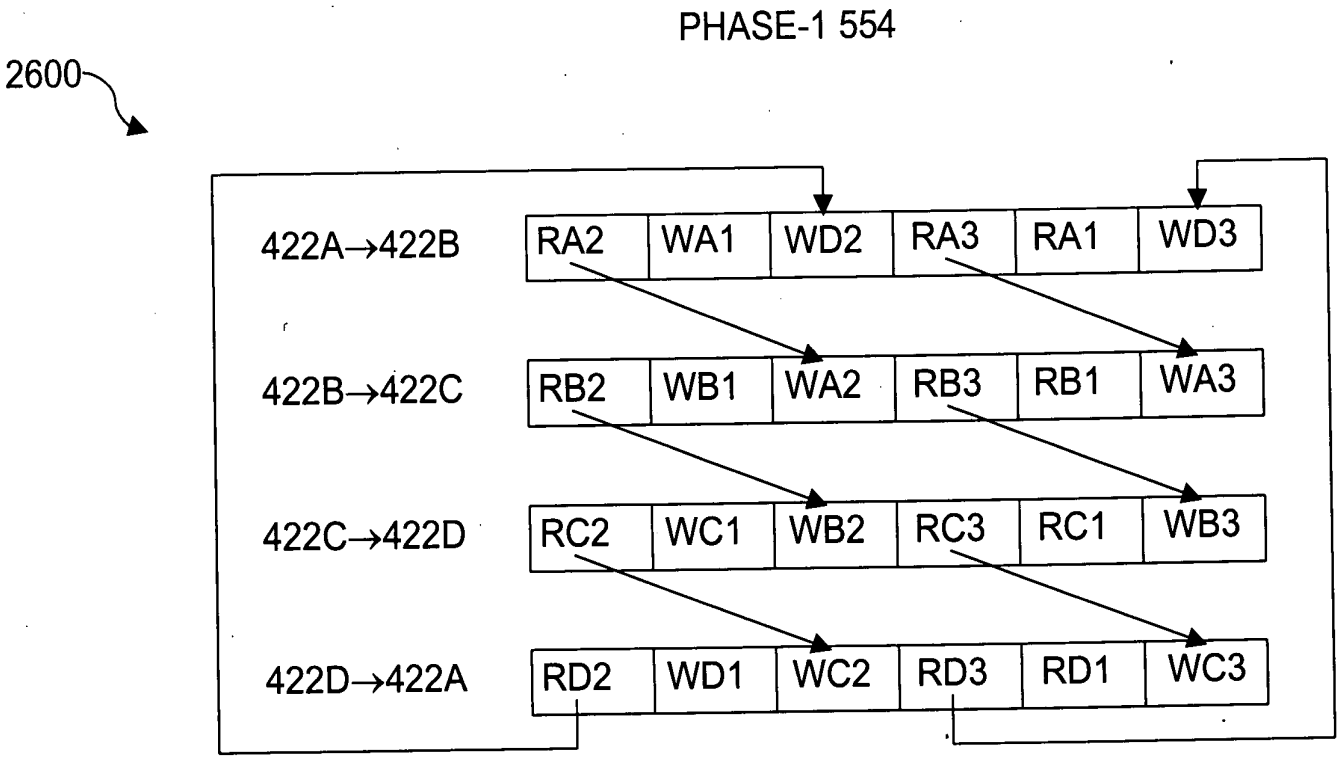

PHASE-1 554
2600
422A→422B
RA2
WA1
WD2
RA3
RA1
WD3
422B→422C
RB2
WB1
WA2
RB3
RB1
WA3
422C→422D
RC2
WC1
WB2
RC3
RC1
WB3
422D→422A
RD2
WD1
WC2
RD3
RD1
WC3

FIG. 26

2701

	PHASE							
	0	*1*	*2*	*3*	*4*	*5*	*6*	7
MODULE RECEIVING FROM MODULE 2	2	3	4	5	6	7	0	1
MODULE TRANSMITTING TO MODULE 0	0	7	6	5	4	3	2	1

2704
2706
2708

2702

	INTERMEDIATE MODULE							
	0	*1*	*2*	*3*	*4*	*5*	*6*	7
DATA SEGMENT RECEIPT PHASE	×	7	×	1	2	3	4	5
DATA SEGMENT TRANSMIT PHASE	×	7	×	5	4	3	2	1
DELAY	×	8	×	4	2	8	6	4

2710
2712
2714
2716

FIG. 27

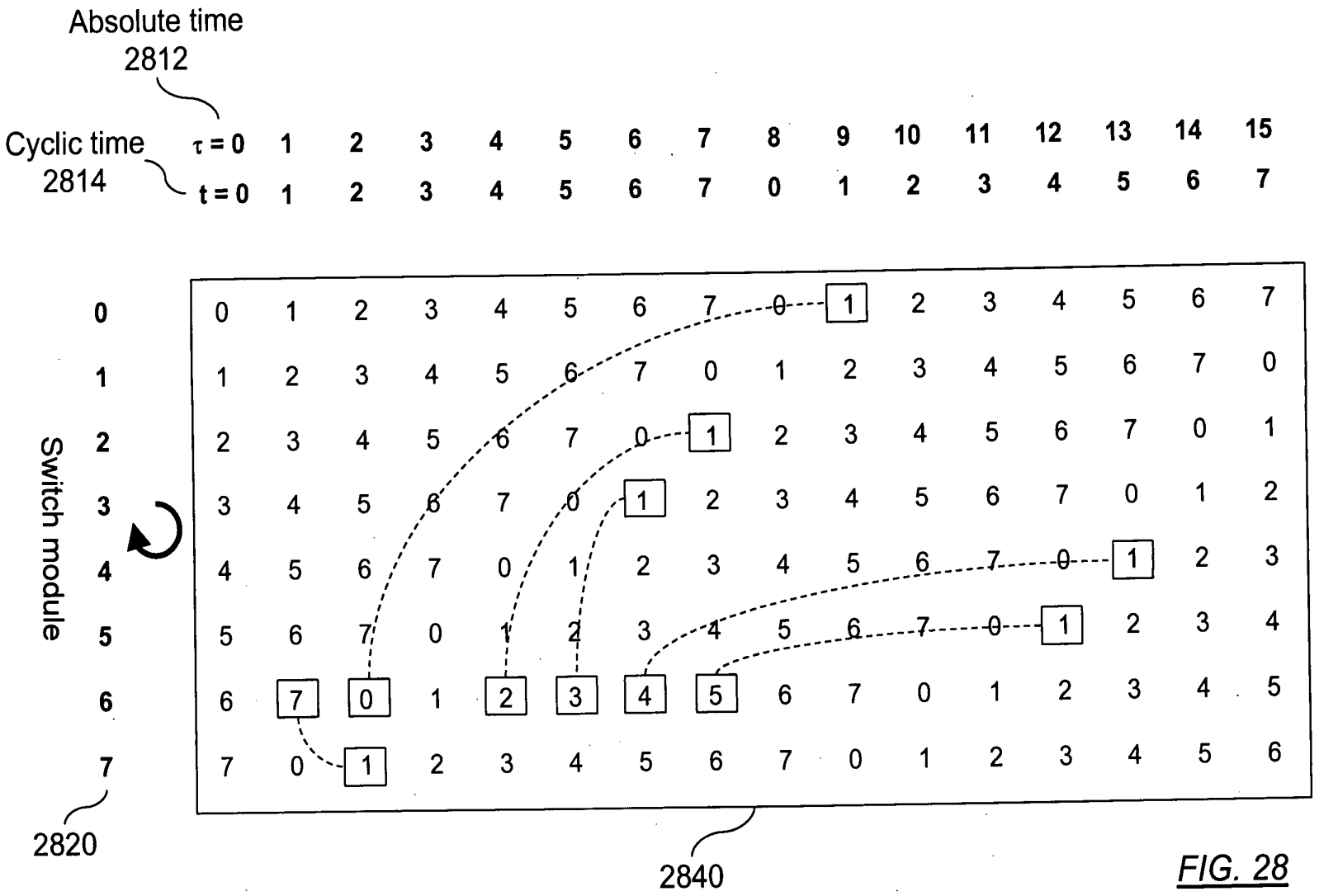

Absolute time
2812
Cyclic time
2814
τ = 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
t = 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7
Switch module
0
1
2
3
4
5
6
7
2820
2840

FIG. 28

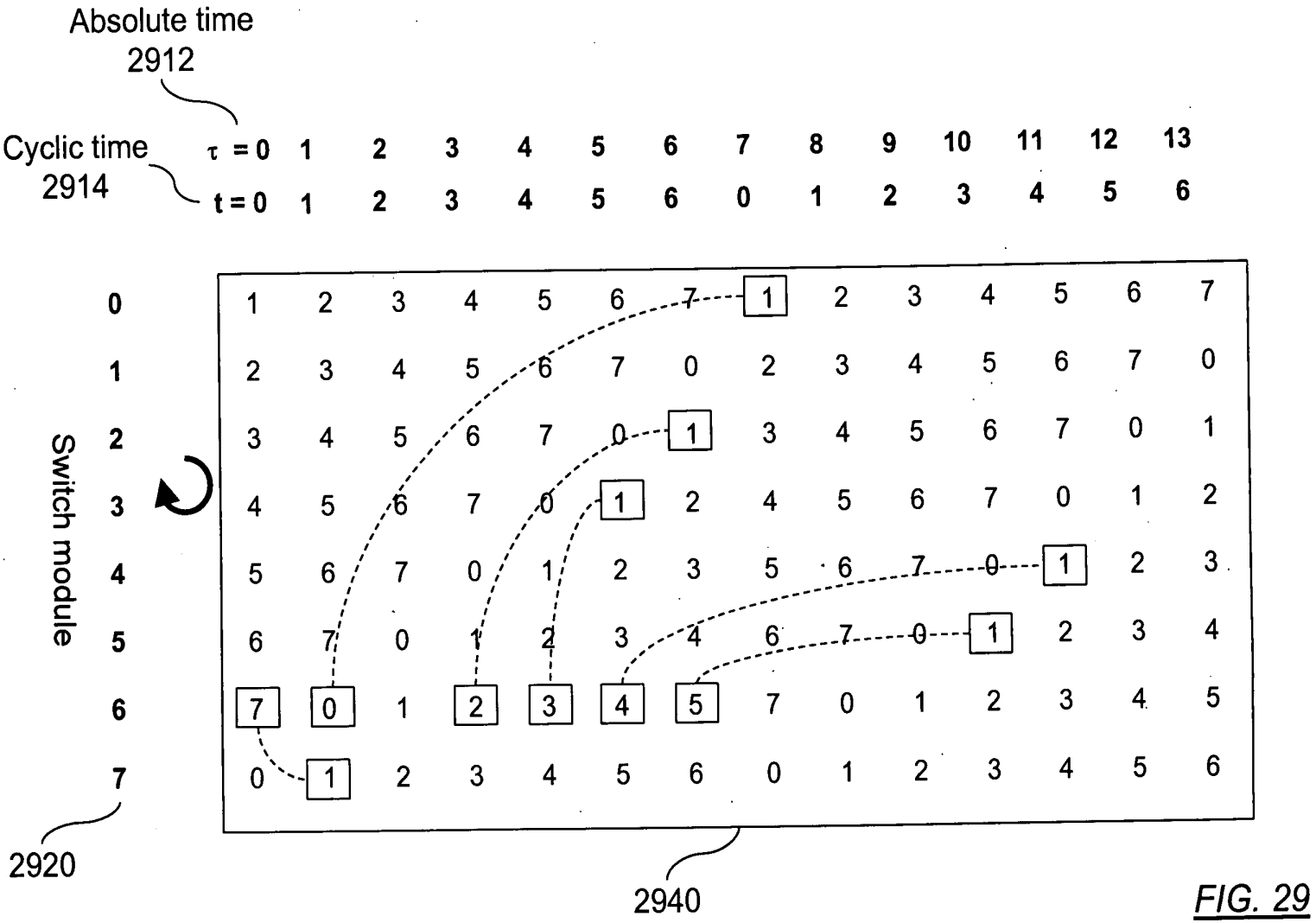

Absolute time
2912
Cyclic time
2914
τ = 0 1 2 3 4 5 6 7 8 9 10 11 12 13
t = 0 1 2 3 4 5 6 0 1 2 3 4 5 6
Switch module
0
1
2
3
4
5
6
7
2920
2940

FIG. 29

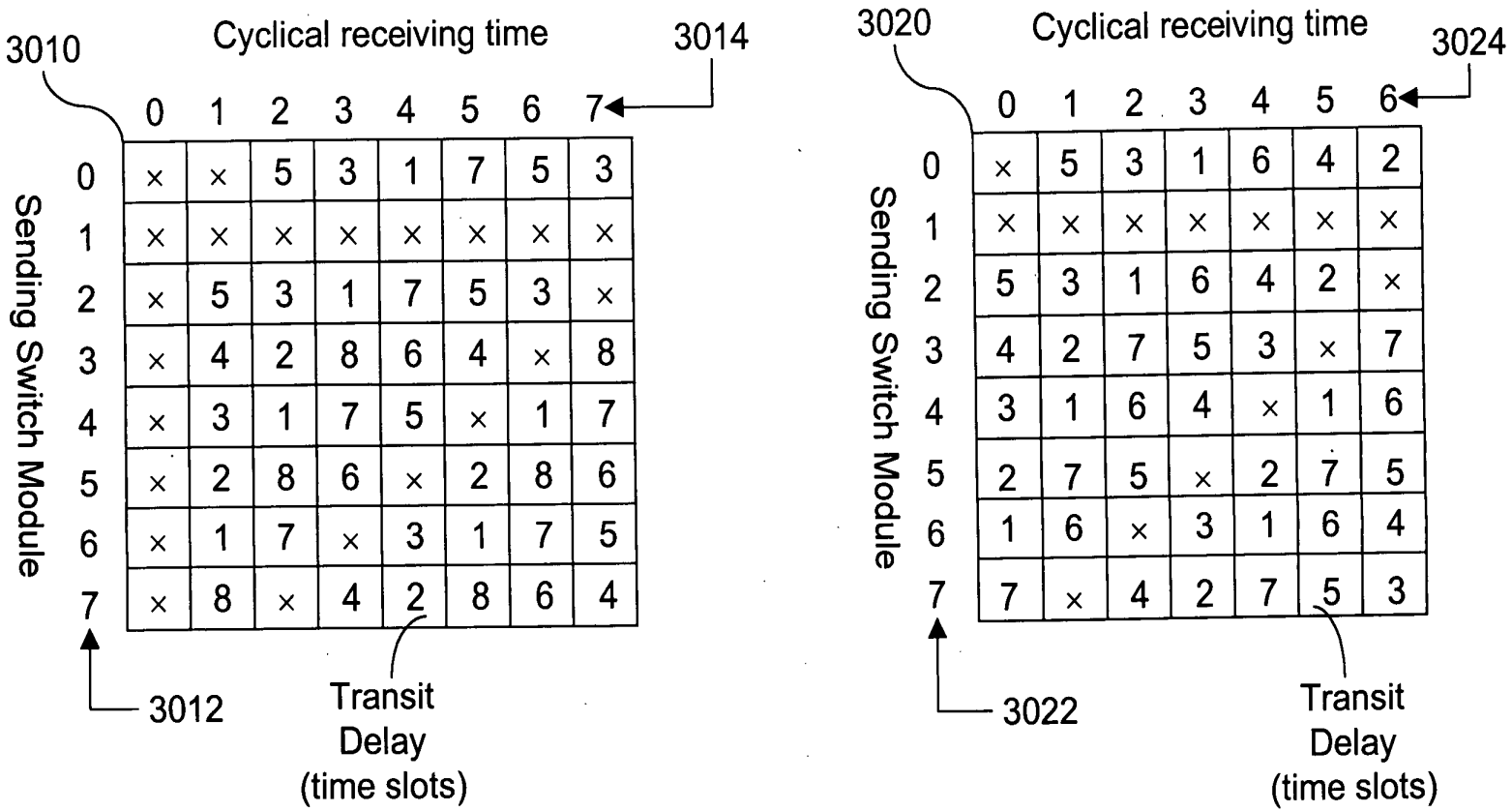

3010
Cyclical receiving time
3014
0 1 2 3 4 5 6 7
Sending Switch Module
0 × × 5 3 1 7 5 3
1 × × × × × × × ×
2 × 5 3 1 7 5 3 ×
3 × 4 2 8 6 4 × 8
4 × 3 1 7 5 × 1 7
5 × 2 8 6 × 2 8 6
6 × 1 7 × 3 1 7 5
7 × 8 × 4 2 8 6 4
3012
Transit Delay (time slots)
3020
Cyclical receiving time
3024
0 1 2 3 4 5 6
Sending Switch Module
0 × 5 3 1 6 4 2
1 × × × × × × ×
2 5 3 1 6 4 2 ×
3 4 2 7 5 3 × 7
4 3 1 6 4 × 1 6
5 2 7 5 × 2 7 5
6 1 6 × 3 1 6 4
7 7 × 4 2 7 5 3
3022
Transit Delay (time slots)

FIG. 30

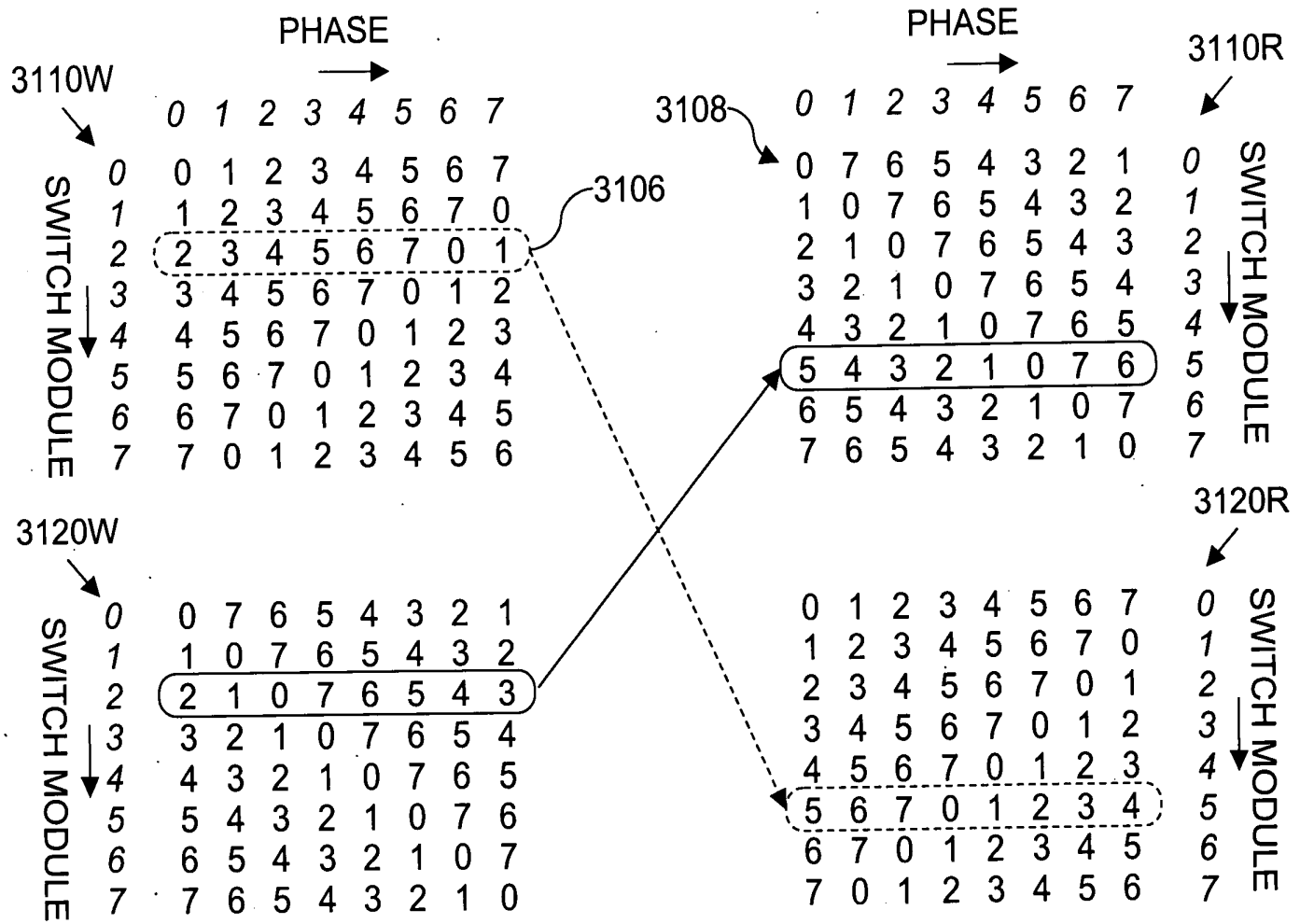

PHASE
3110W
SWITCH MODULE
3106
3120W
SWITCH MODULE
PHASE
3108
3110R
SWITCH MODULE
3120R
SWITCH MODULE

FIG. 31

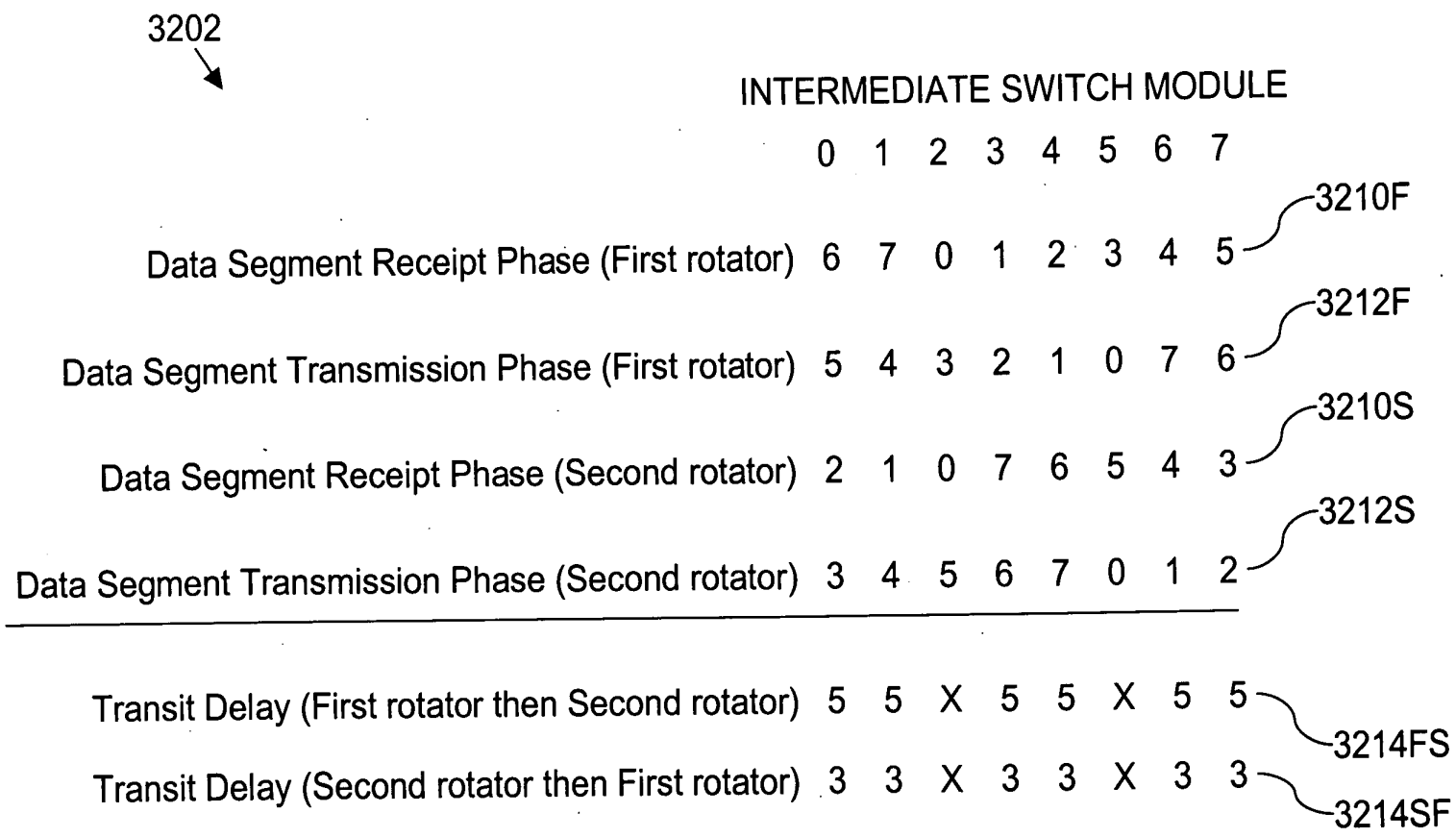

3202
INTERMEDIATE SWITCH MODULE
0 1 2 3 4 5 6 7
Data Segment Receipt Phase (First rotator) 6 7 0 1 2 3 4 5
3210F
Data Segment Transmission Phase (First rotator) 5 4 3 2 1 0 7 6
3212F
Data Segment Receipt Phase (Second rotator) 2 1 0 7 6 5 4 3
3210S
Data Segment Transmission Phase (Second rotator) 3 4 5 6 7 0 1 2
3212S
Transit Delay (First rotator then Second rotator) 5 5 X 5 5 X 5 5
3214FS
Transit Delay (Second rotator then First rotator) 3 3 X 3 3 X 3 3
3214SF

FIG. 32

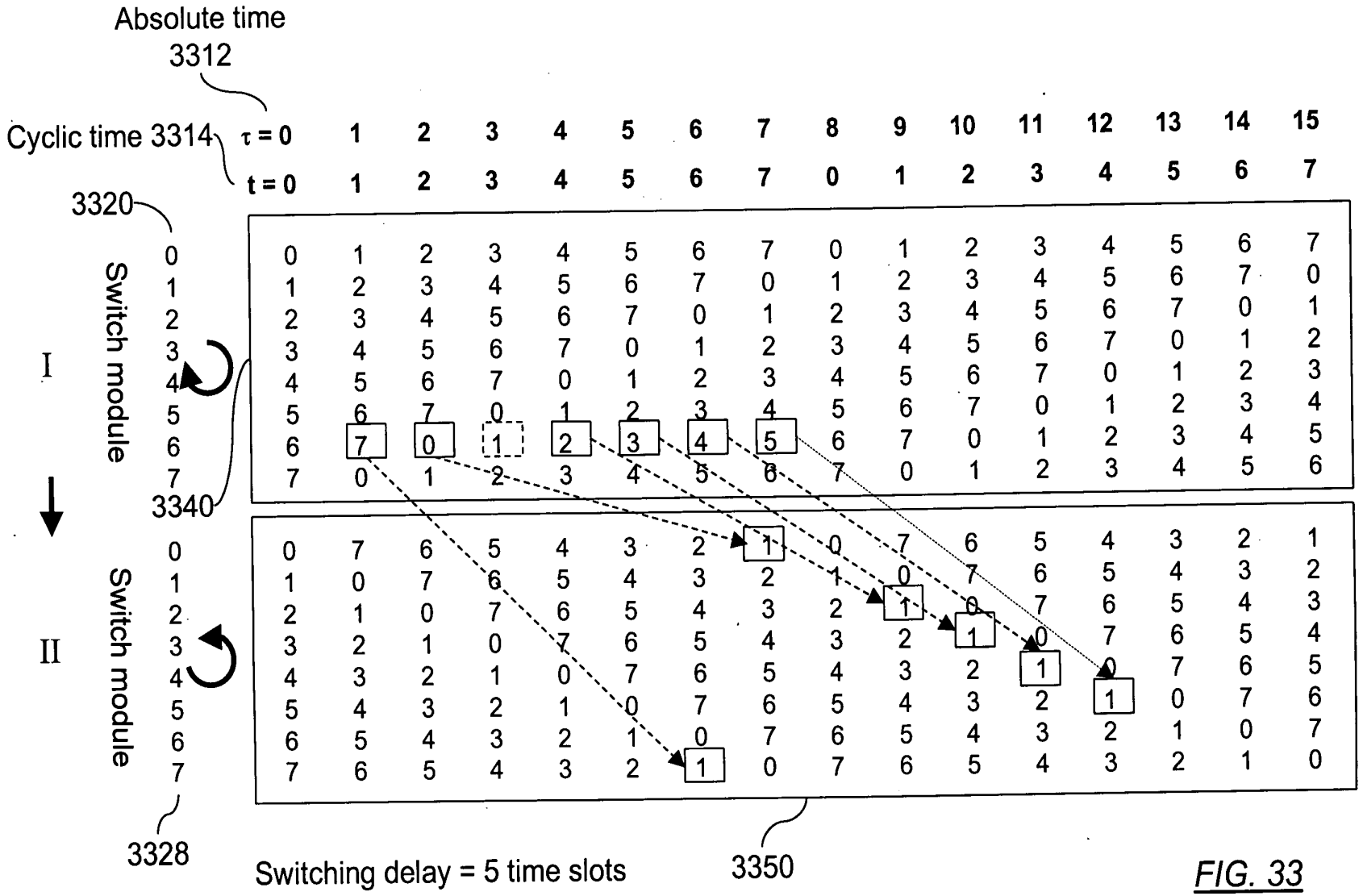

Absolute time
3312
Cyclic time 3314
τ = 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
t = 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7
3320
I
Switch module
II
Switch module
3340
3328
3350
Switching delay = 5 time slots

FIG. 33

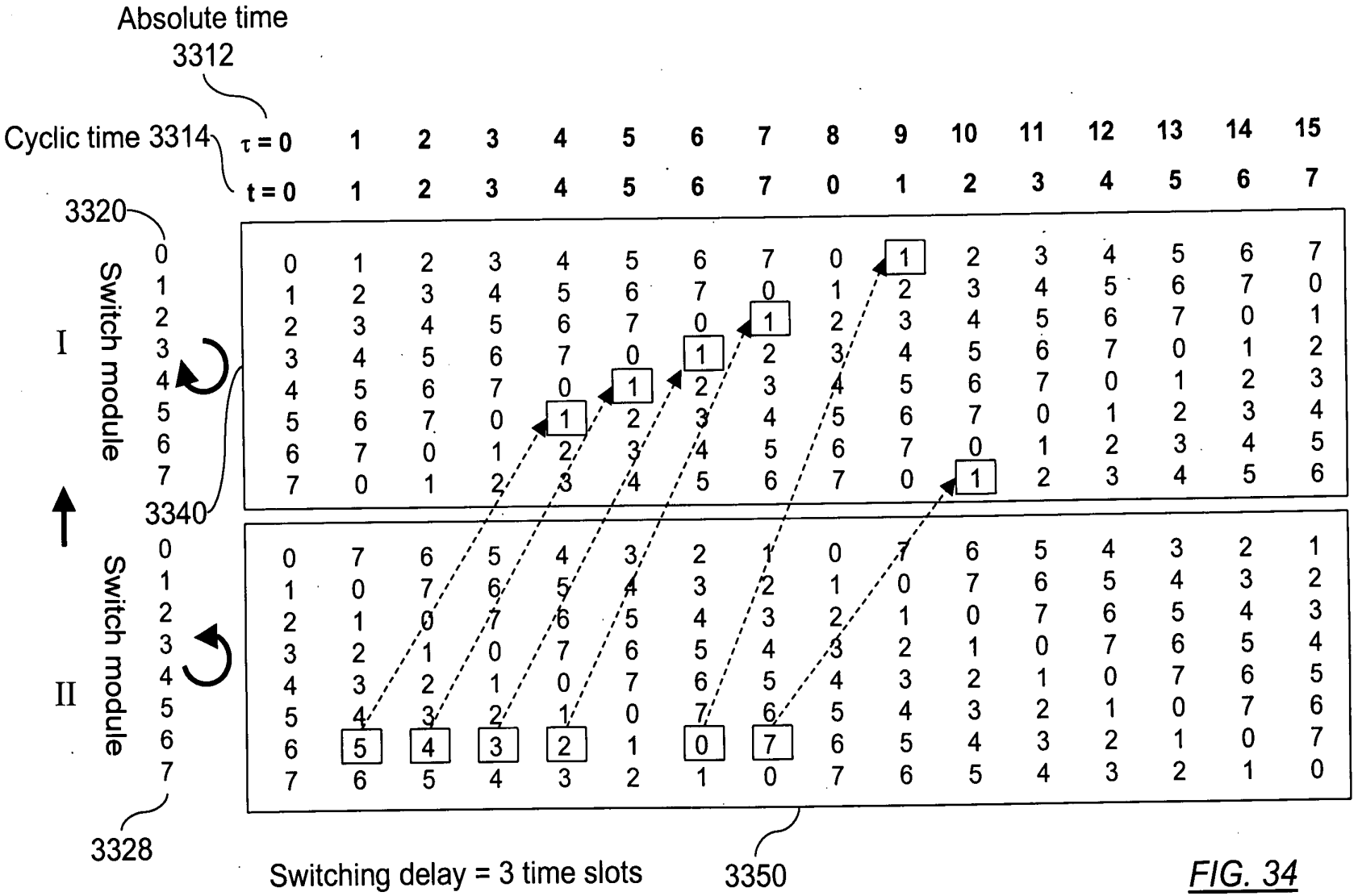

Absolute time
3312
Cyclic time 3314
τ = 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
t = 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7
3320
I
Switch module
II
Switch module
3340
3328
Switching delay = 3 time slots
3350

FIG. 34

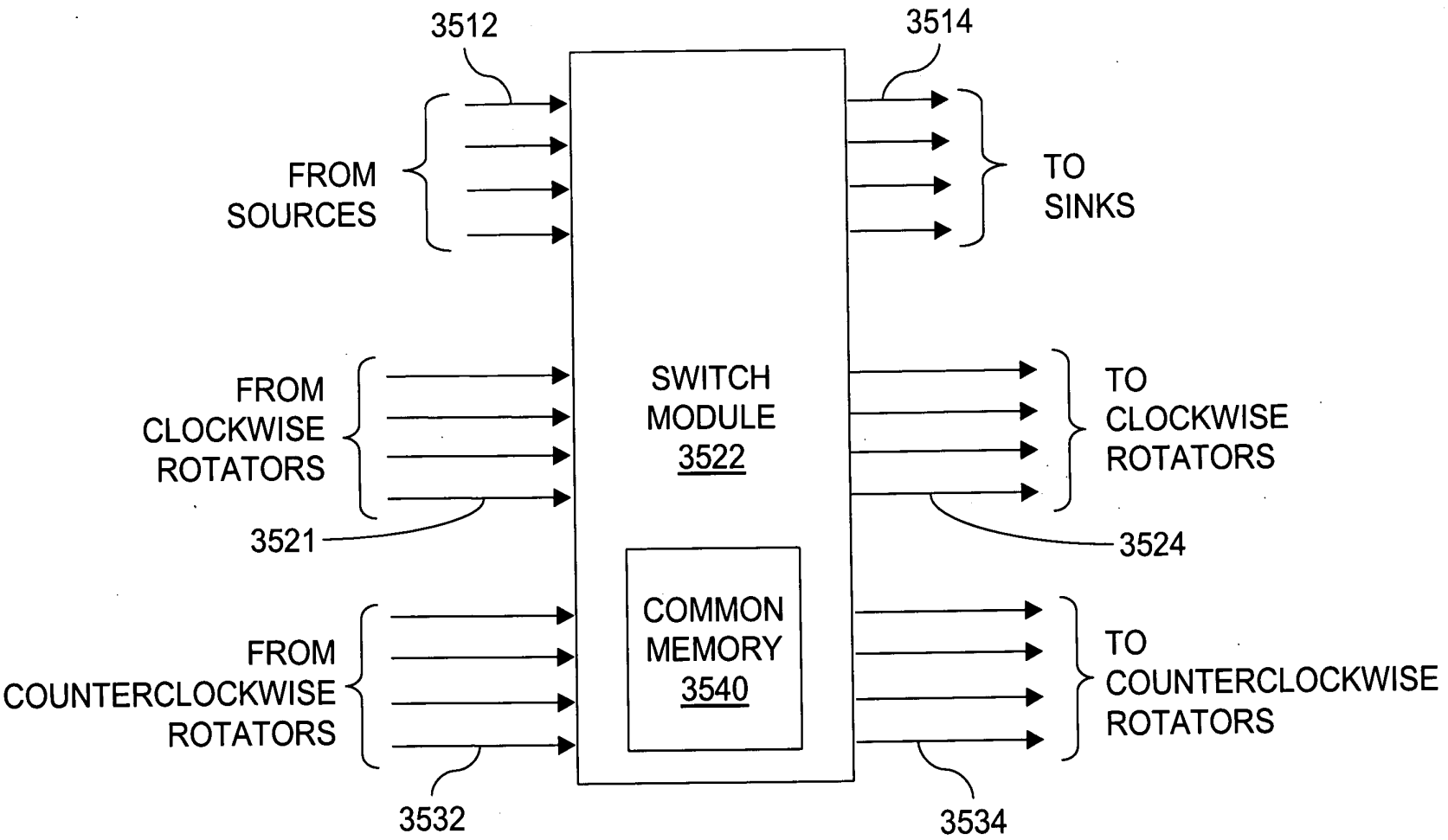

3512
3514
FROM
SOURCES
TO
SINKS
FROM
CLOCKWISE
ROTATORS
SWITCH
MODULE
3522
TO
CLOCKWISE
ROTATORS
3521
3524
COMMON
MEMORY
3540
FROM
COUNTERCLOCKWISE
ROTATORS
TO
COUNTERCLOCKWISE
ROTATORS
3532
3534

FIG. 35

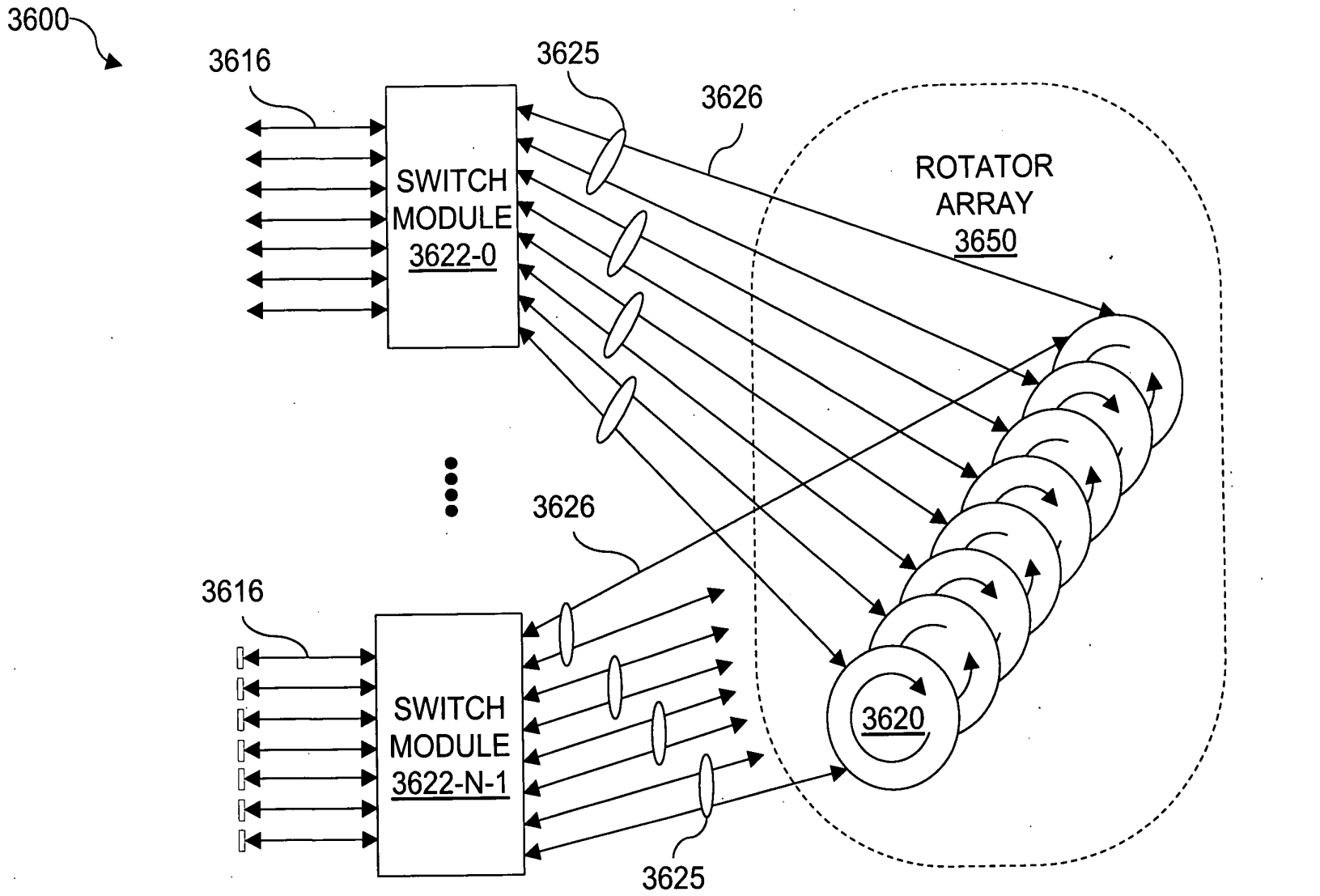

3600
3616
3625
3626
SWITCH MODULE 3622-0
ROTATOR ARRAY 3650
3626
3616
SWITCH MODULE 3622-N-1
3620
3625

FIG. 36

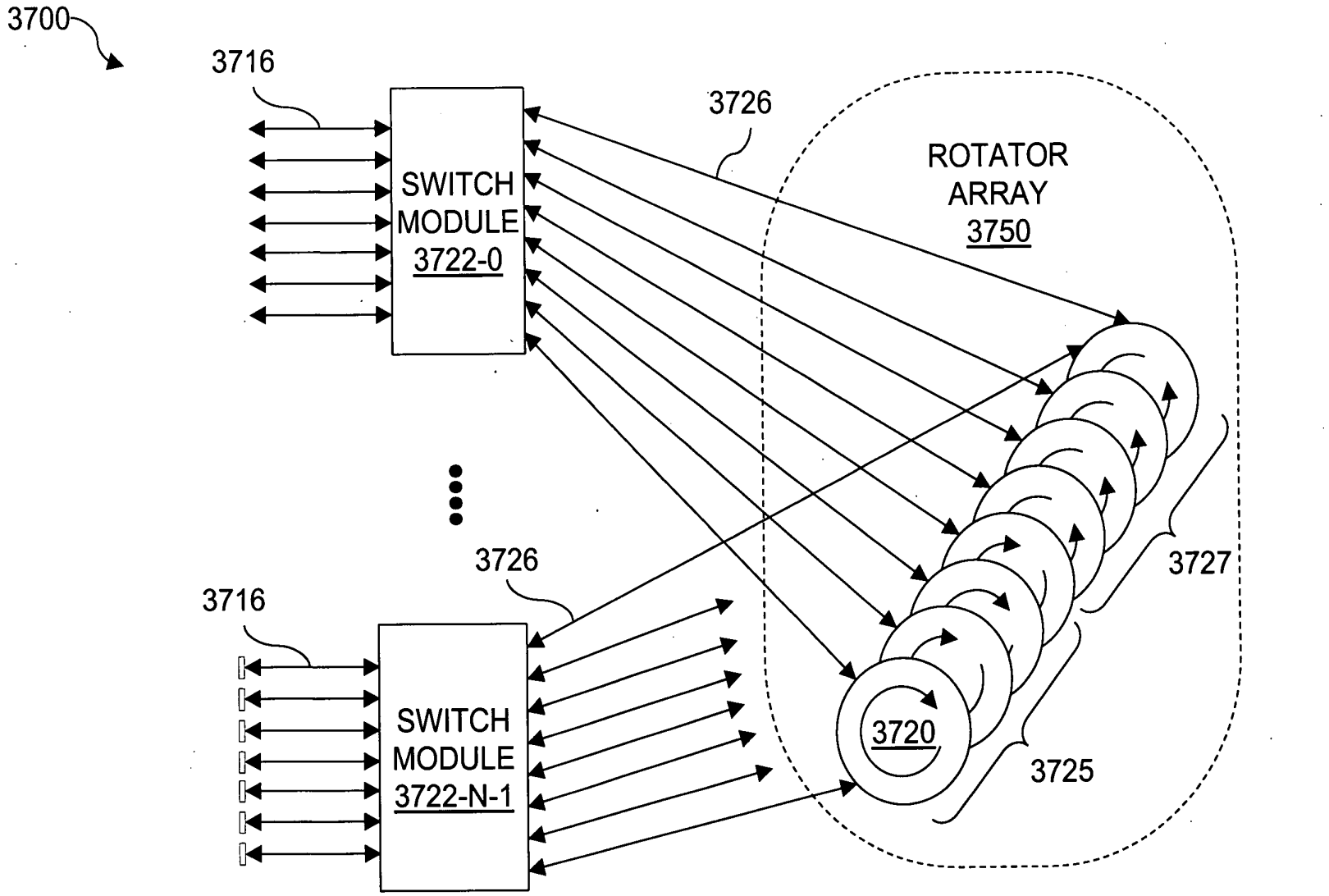

3700
3716
SWITCH MODULE 3722-0
3726
ROTATOR ARRAY 3750
3727
3716
SWITCH MODULE 3722-N-1
3726
3720
3725

FIG. 37

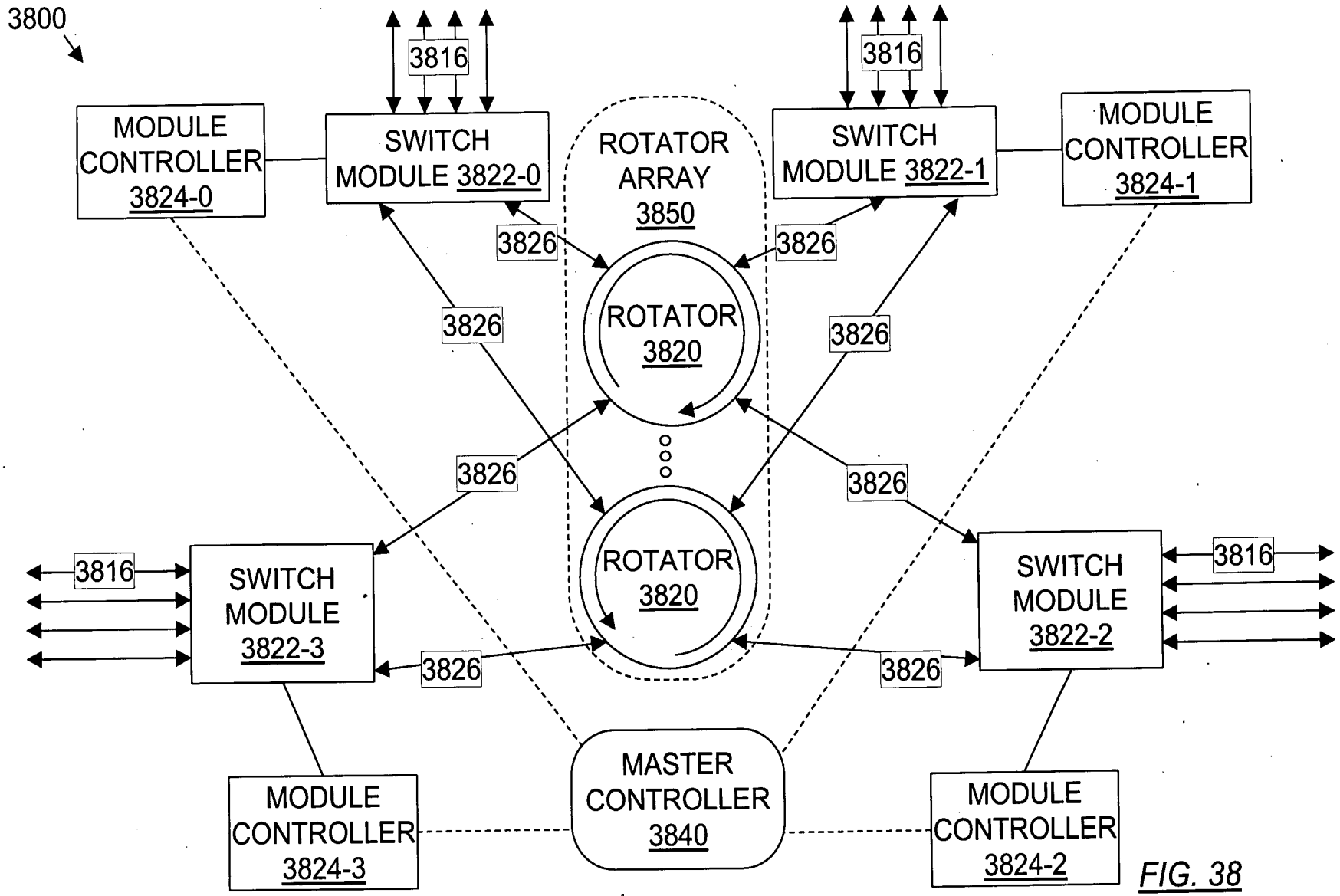

3800
3816
3816
MODULE CONTROLLER 3824-0
SWITCH MODULE 3822-0
ROTATOR ARRAY 3850
SWITCH MODULE 3822-1
MODULE CONTROLLER 3824-1
3826
3826
3826
3826
ROTATOR 3820
3826
3826
ROTATOR 3820
3816
SWITCH MODULE 3822-3
SWITCH MODULE 3822-2
3816
3826
3826
MASTER CONTROLLER 3840
MODULE CONTROLLER 3824-3
MODULE CONTROLLER 3824-2

FIG. 38

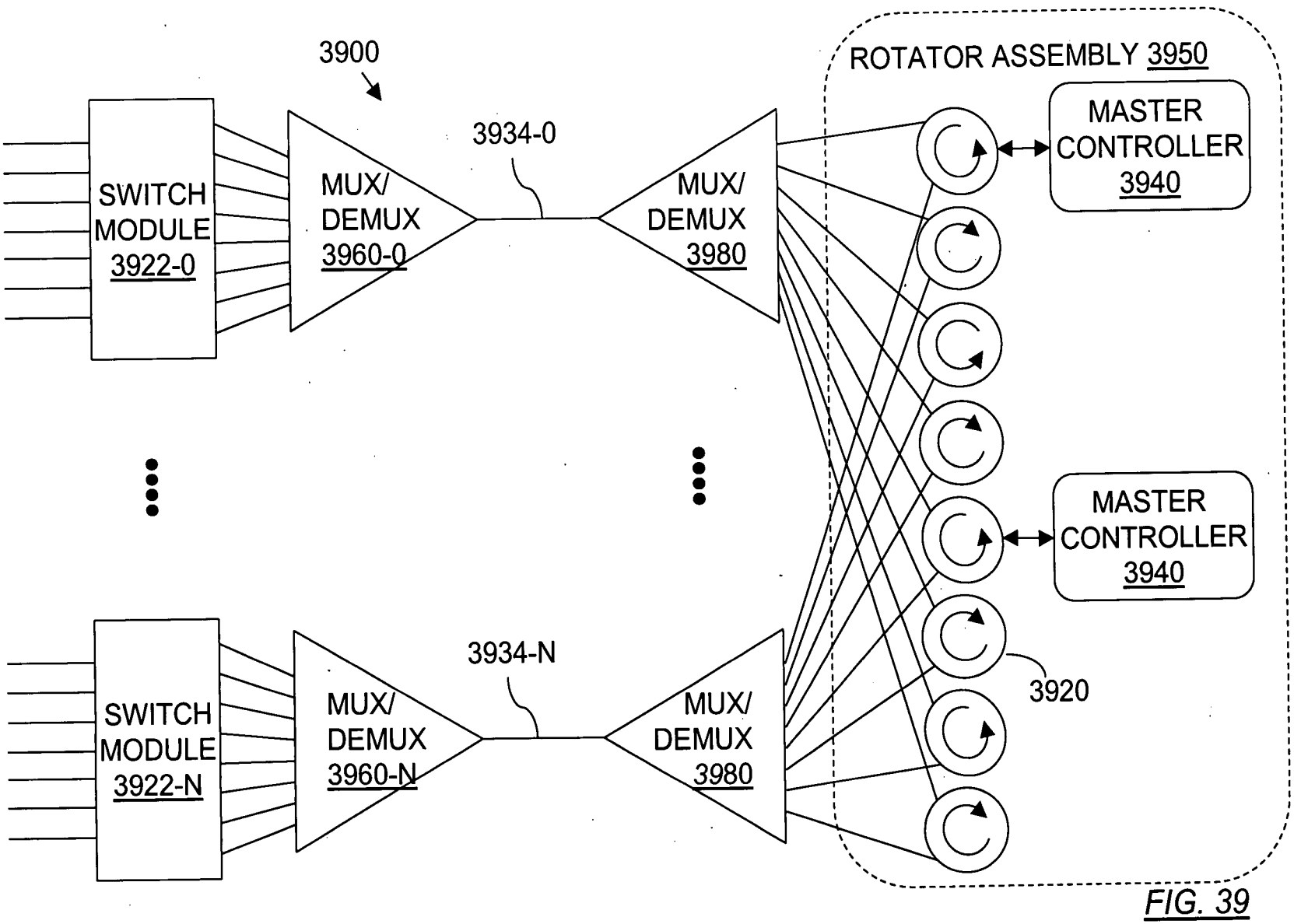

3900
ROTATOR ASSEMBLY 3950
SWITCH MODULE 3922-0
MUX/ DEMUX 3960-0
3934-0
MUX/ DEMUX 3980
MASTER CONTROLLER 3940
MASTER CONTROLLER 3940
SWITCH MODULE 3922-N
MUX/ DEMUX 3960-N
3934-N
MUX/ DEMUX 3980
3920

FIG. 39

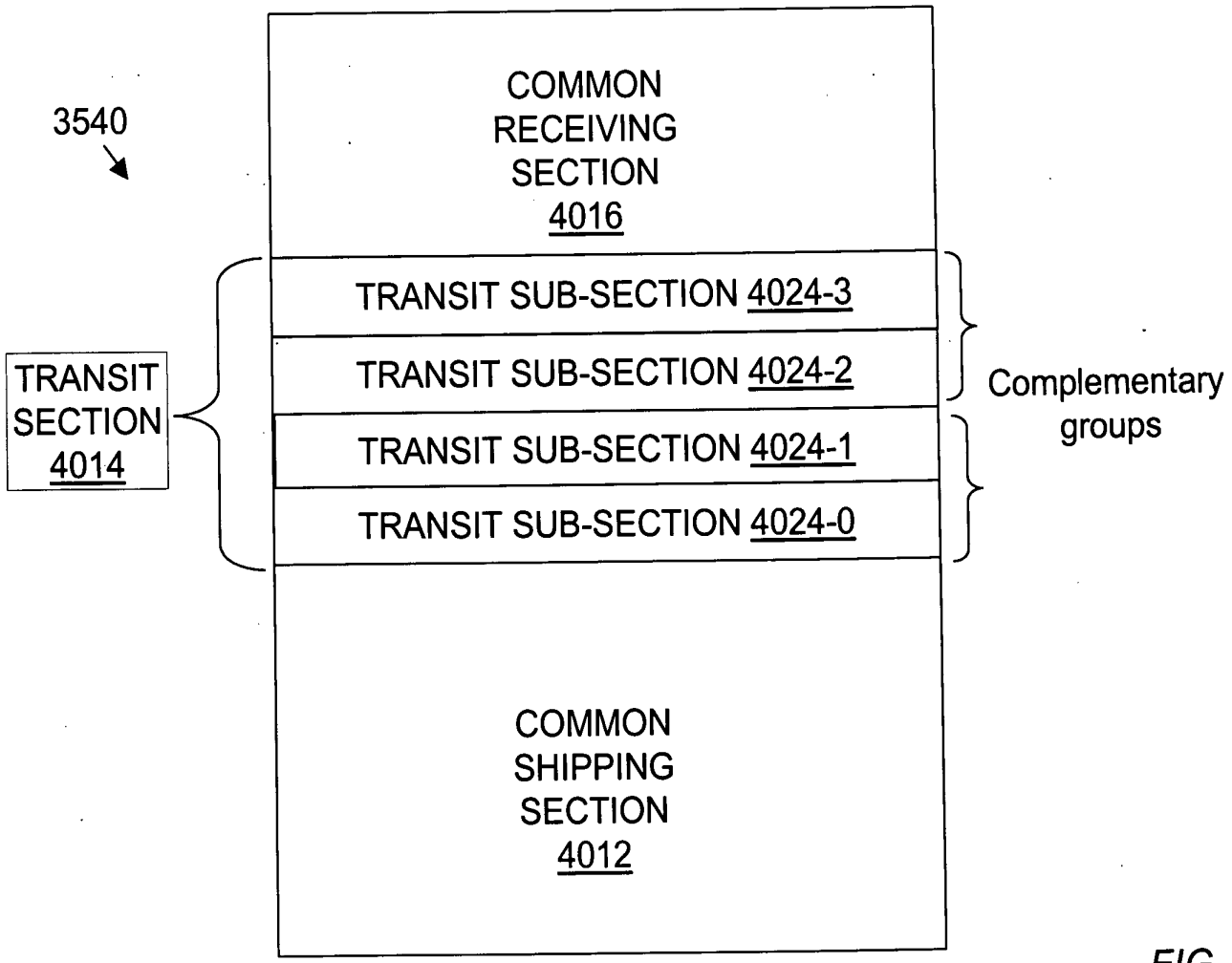

3540
COMMON RECEIVING SECTION 4016
TRANSIT SUB-SECTION 4024-3
TRANSIT SUB-SECTION 4024-2
TRANSIT SUB-SECTION 4024-1
TRANSIT SUB-SECTION 4024-0
TRANSIT SECTION 4014
Complementary groups
COMMON SHIPPING SECTION 4012

FIG. 40

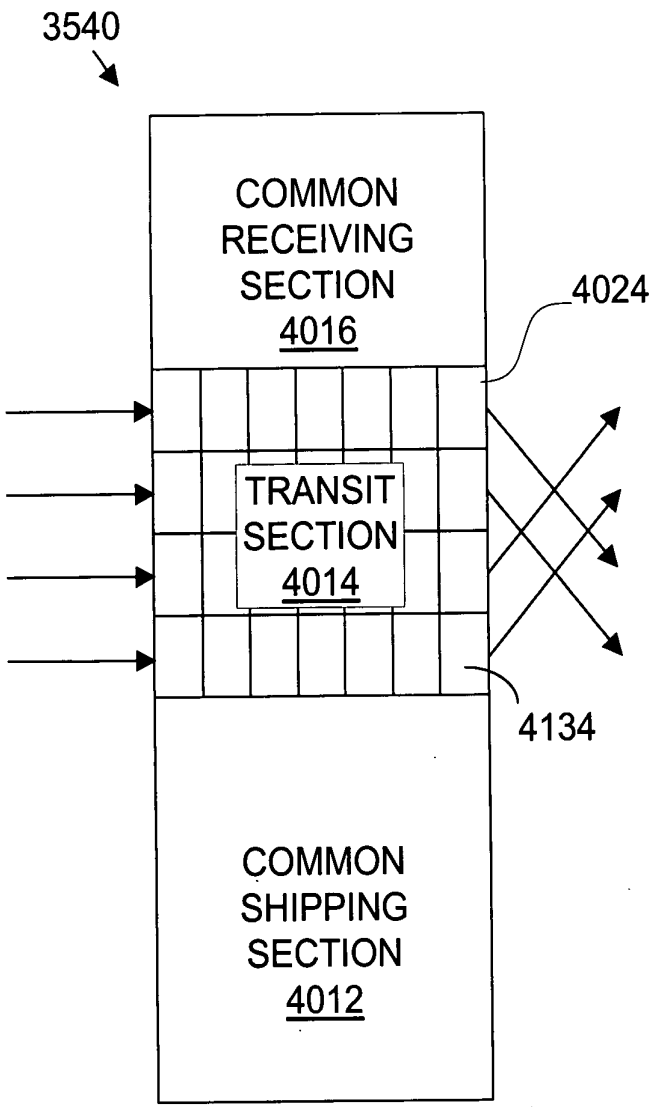


FIG. 41A

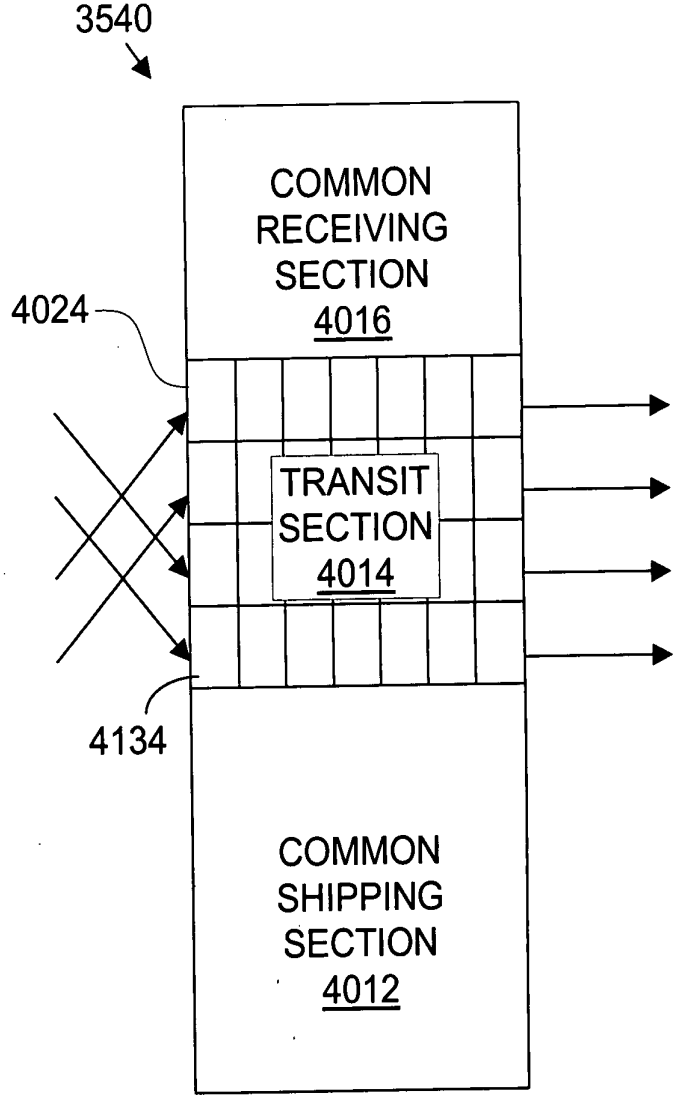


FIG. 41B

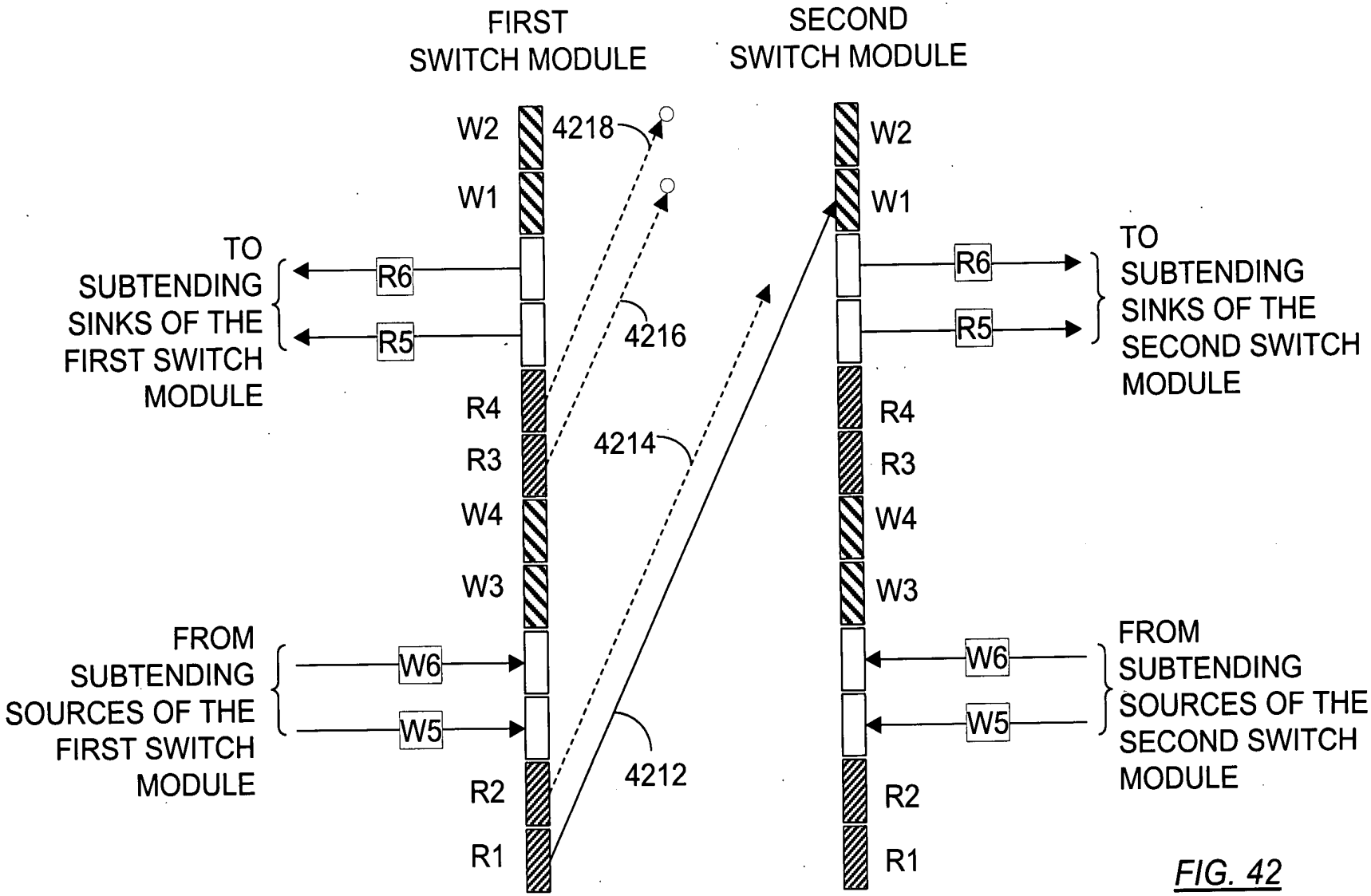

FIRST
SWITCH MODULE
SECOND
SWITCH MODULE
W2
W1
R6
R5
R4
R3
W4
W3
W6
W5
R2
R1
4218
4216
4214
4212
TO
SUBTENDING
SINKS OF THE
FIRST SWITCH
MODULE
FROM
SUBTENDING
SOURCES OF THE
FIRST SWITCH
MODULE
TO
SUBTENDING
SINKS OF THE
SECOND SWITCH
MODULE
FROM
SUBTENDING
SOURCES OF THE
SECOND SWITCH
MODULE

FIG. 42

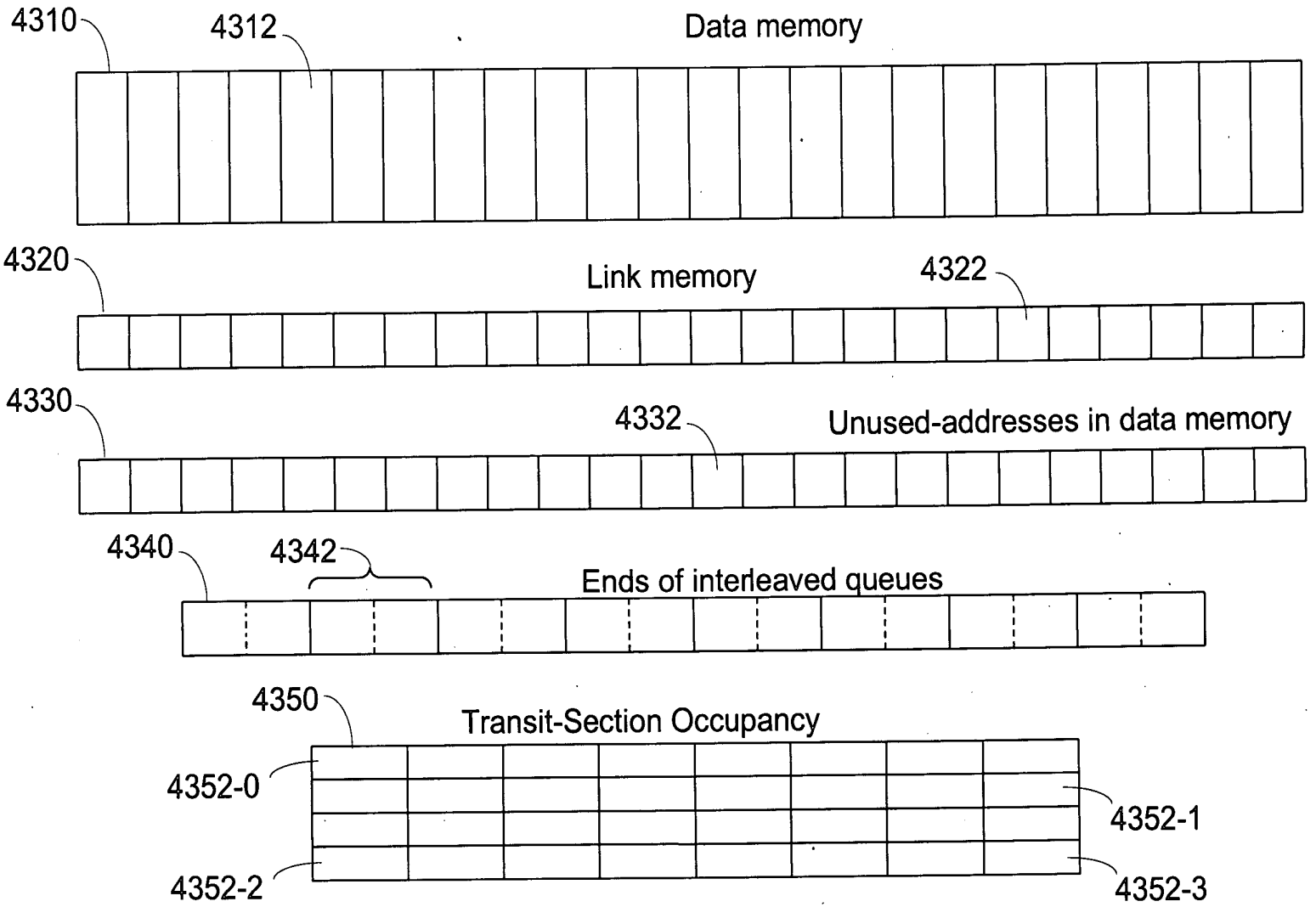

4310
4312
Data memory
4320
Link memory
4322
4330
4332
Unused-addresses in data memory
4340
4342
Ends of interleaved queues
4350
Transit-Section Occupancy
4352-0
4352-1
4352-2
4352-3

FIG. 43

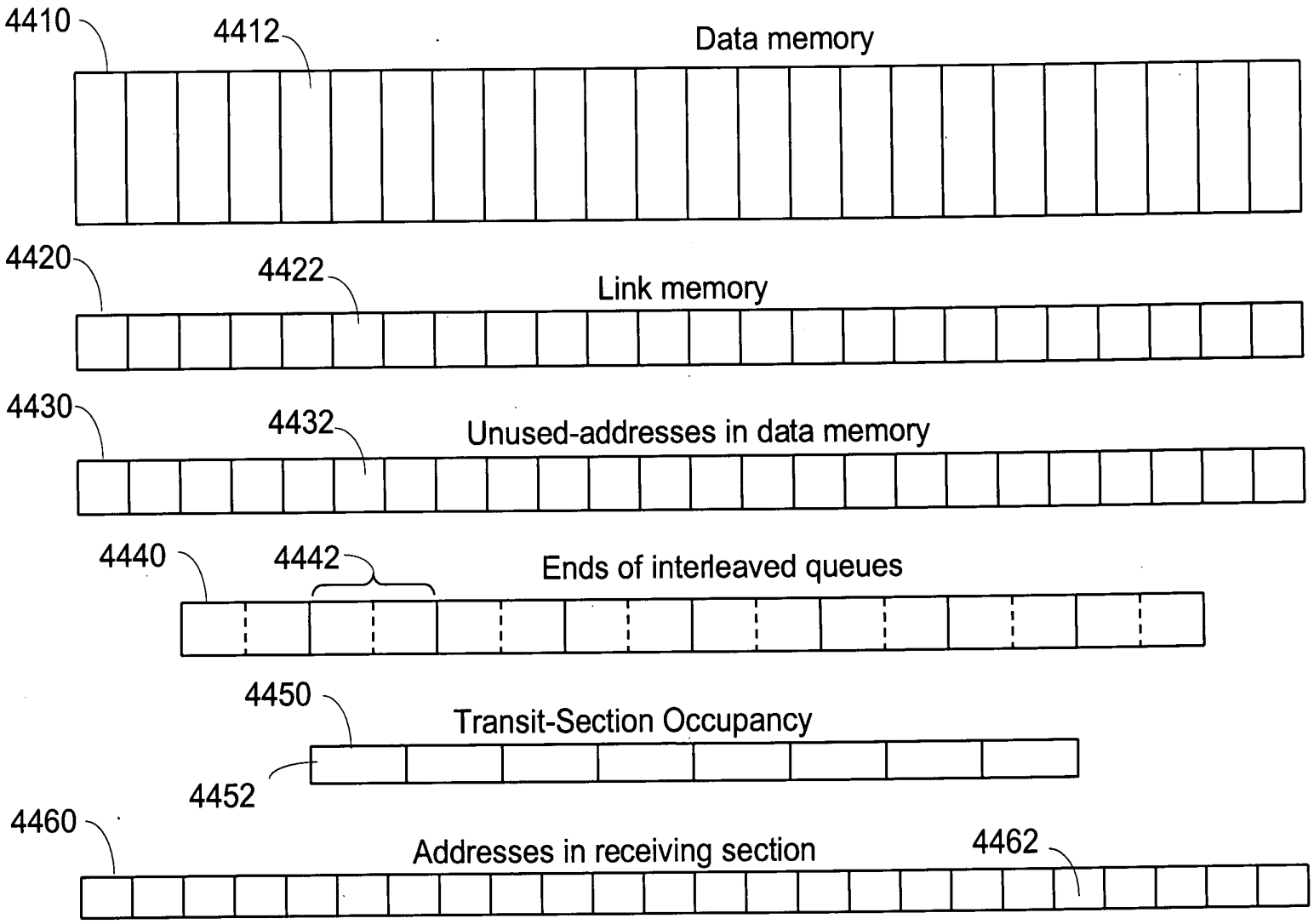

4410
4412
Data memory
4420
4422
Link memory
4430
4432
Unused-addresses in data memory
4440
4442
Ends of interleaved queues
4450
Transit-Section Occupancy
4452
4460
Addresses in receiving section
4462

FIG. 44

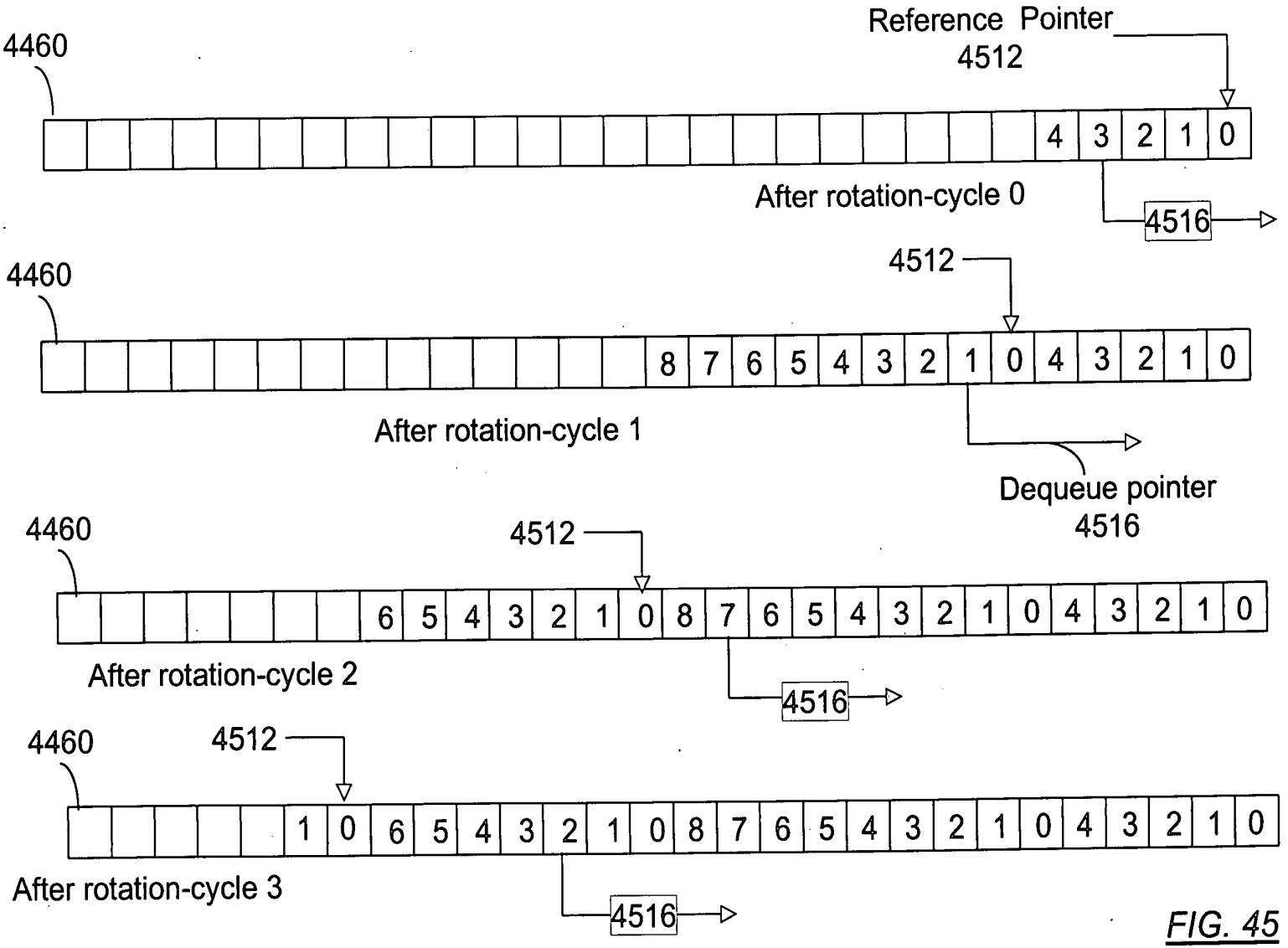

4460
Reference Pointer
4512
4 3 2 1 0
After rotation-cycle 0
4516
4460
4512
8 7 6 5 4 3 2 1 0 4 3 2 1 0
After rotation-cycle 1
Dequeue pointer
4516
4460
4512
6 5 4 3 2 1 0 8 7 6 5 4 3 2 1 0 4 3 2 1 0
After rotation-cycle 2
4516
4460
4512
1 0 6 5 4 3 2 1 0 8 7 6 5 4 3 2 1 0 4 3 2 1 0
After rotation-cycle 3
4516

FIG. 45

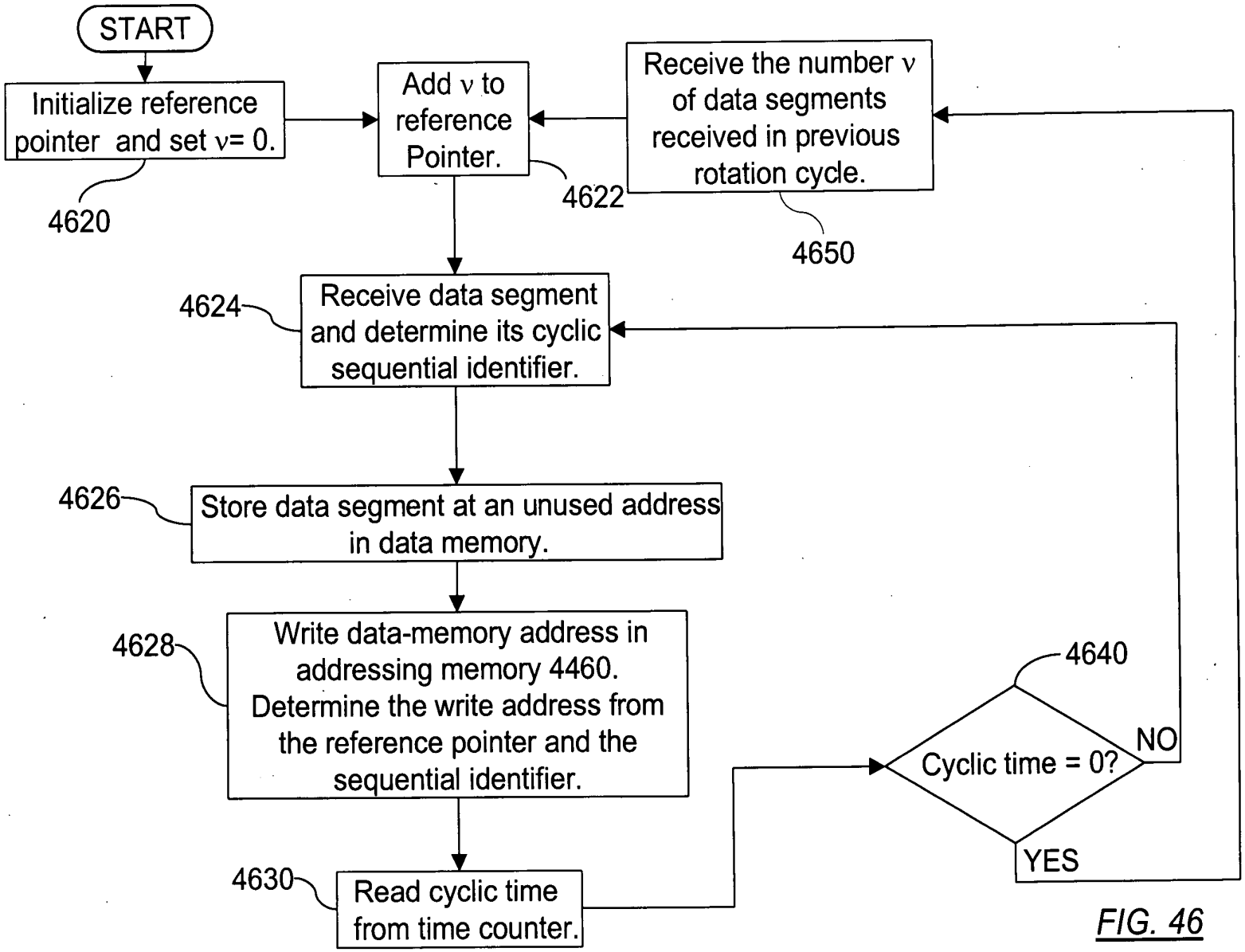

START
Initialize reference pointer and set ν= 0.
4620
Add ν to reference Pointer.
4622
Receive the number ν of data segments received in previous rotation cycle.
4650
4624
Receive data segment and determine its cyclic sequential identifier.
4626
Store data segment at an unused address in data memory.
4628
Write data-memory address in addressing memory 4460. Determine the write address from the reference pointer and the sequential identifier.
4630
Read cyclic time from time counter.
4640
Cyclic time = 0?
NO
YES

FIG. 46

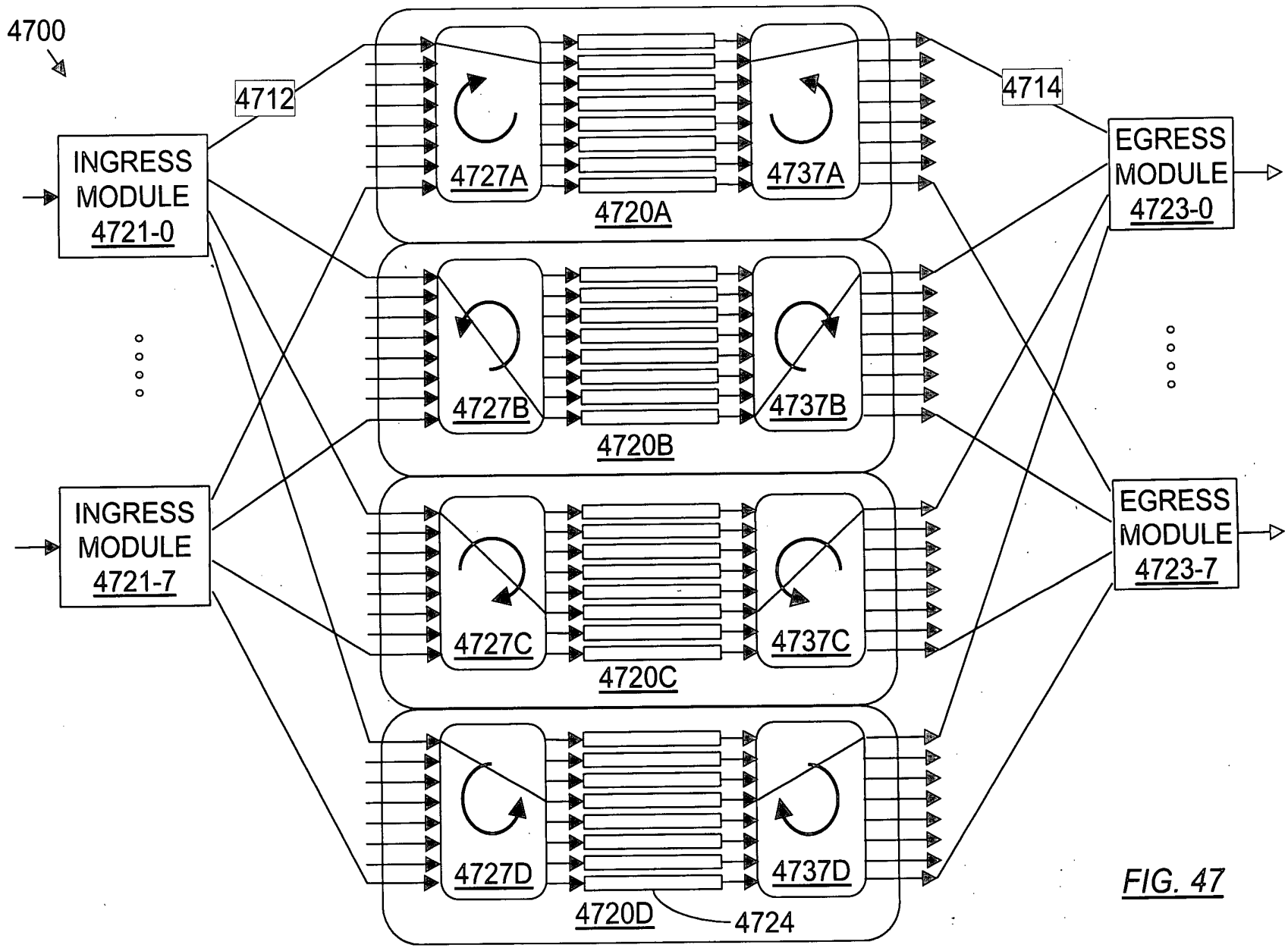

4700
4712
4714
INGRESS MODULE 4721-0
INGRESS MODULE 4721-7
EGRESS MODULE 4723-0
EGRESS MODULE 4723-7
4727A
4737A
4720A
4727B
4737B
4720B
4727C
4737C
4720C
4727D
4737D
4720D
4724

FIG. 47

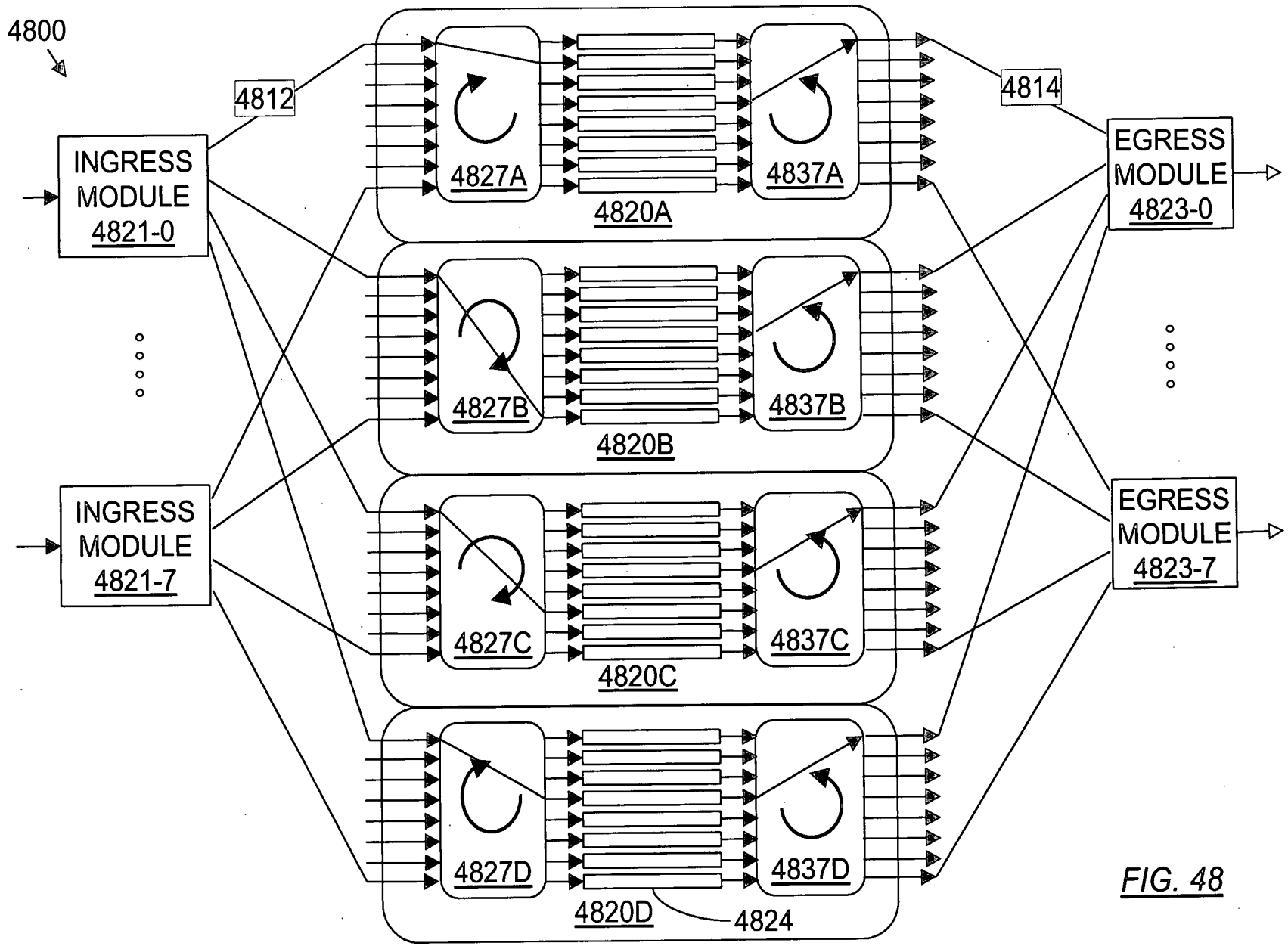

4800
4812
4814
INGRESS MODULE 4821-0
INGRESS MODULE 4821-7
EGRESS MODULE 4823-0
EGRESS MODULE 4823-7
4827A
4837A
4820A
4827B
4837B
4820B
4827C
4837C
4820C
4827D
4837D
4820D
4824

FIG. 48

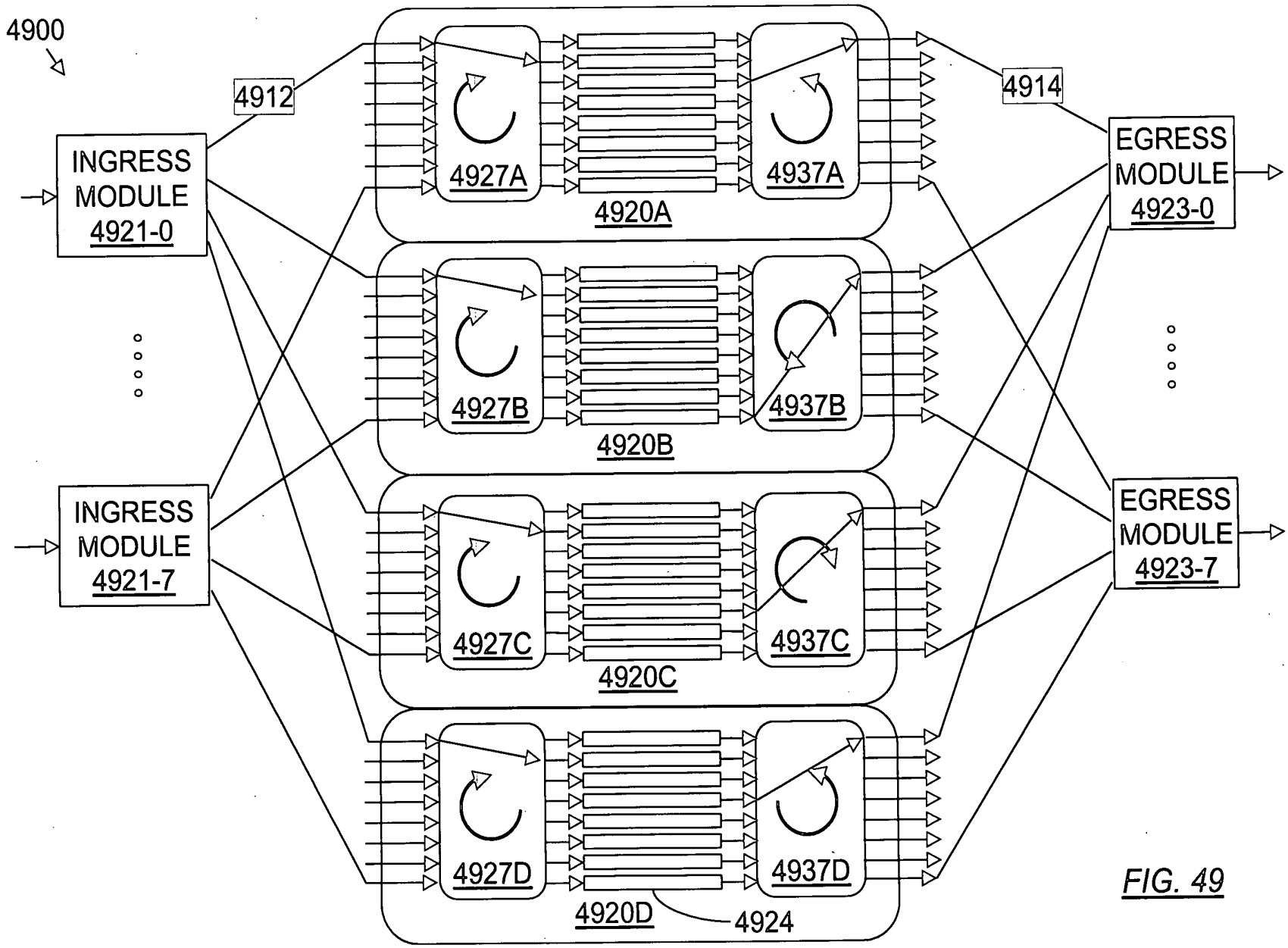

4900
4912
4914
INGRESS MODULE 4921-0
INGRESS MODULE 4921-7
EGRESS MODULE 4923-0
EGRESS MODULE 4923-7
4927A
4937A
4920A
4927B
4937B
4920B
4927C
4937C
4920C
4927D
4937D
4920D
4924

FIG. 49

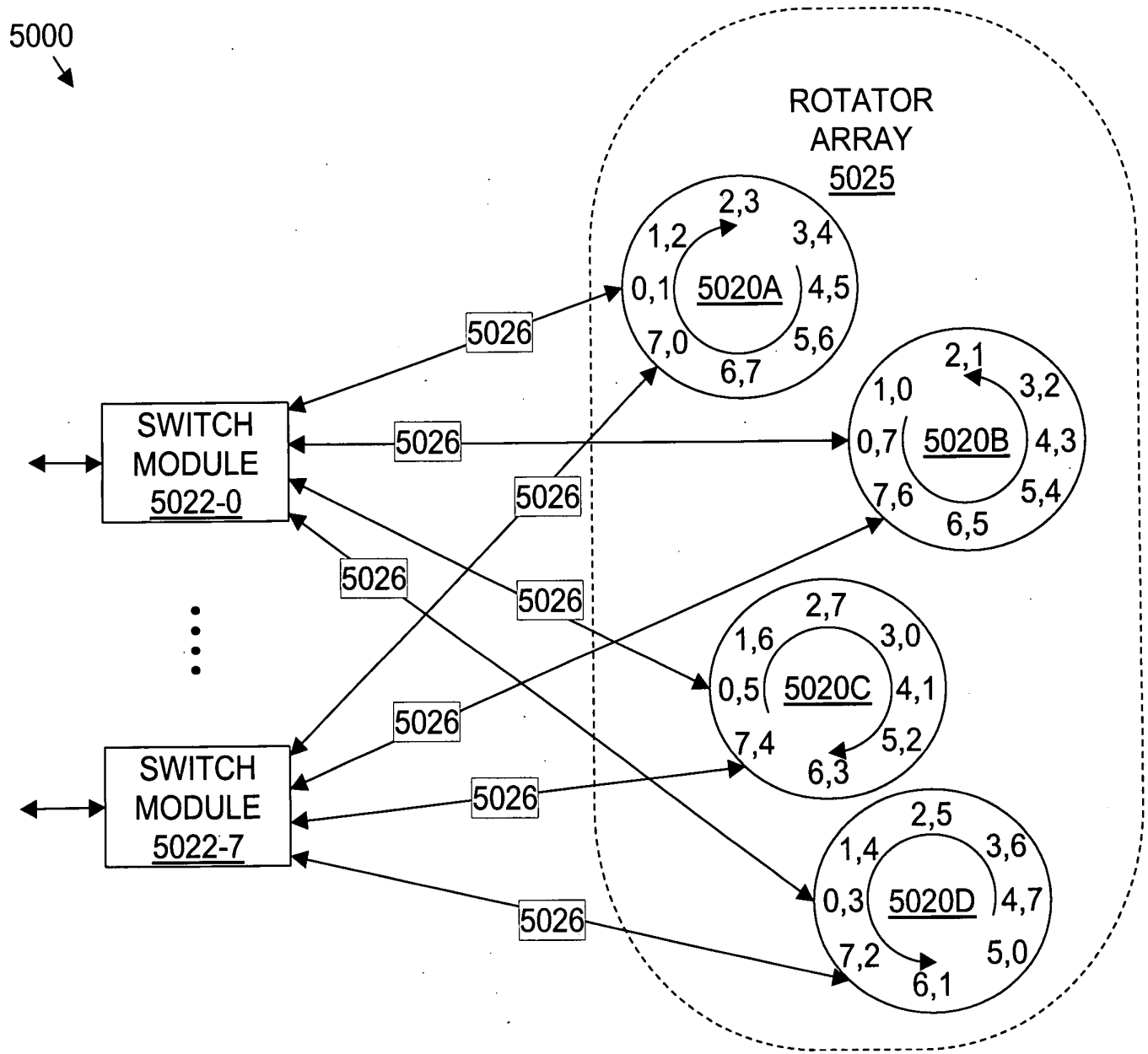

5000
ROTATOR ARRAY 5025
SWITCH MODULE 5022-0
SWITCH MODULE 5022-7
5026
5020A
2,3
1,2
3,4
0,1
4,5
7,0
5,6
6,7
5020B
2,1
1,0
3,2
0,7
4,3
7,6
5,4
6,5
5020C
2,7
1,6
3,0
0,5
4,1
7,4
5,2
6,3
5020D
2,5
1,4
3,6
0,3
4,7
7,2
5,0
6,1

FIG. 50

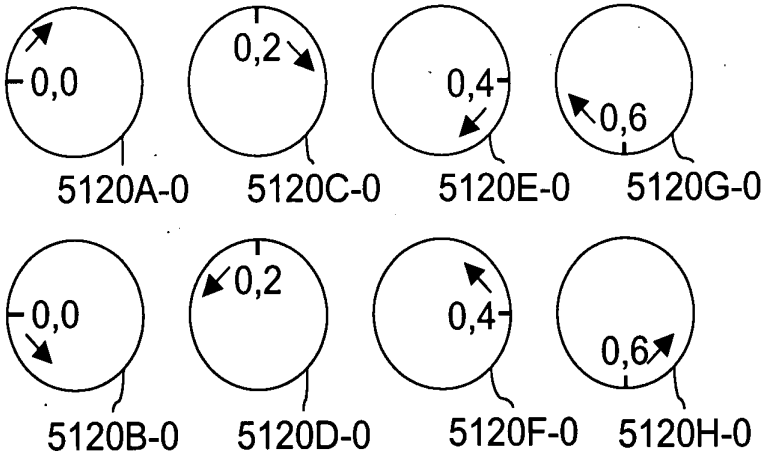


FIG. 51A

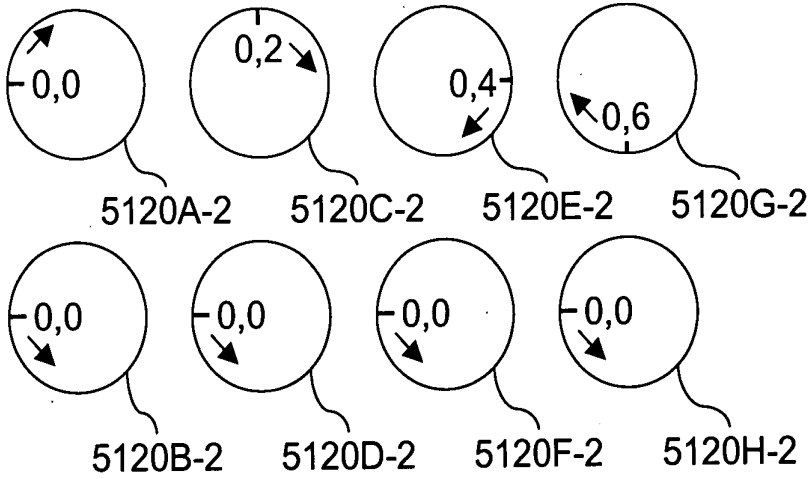


FIG. 51C

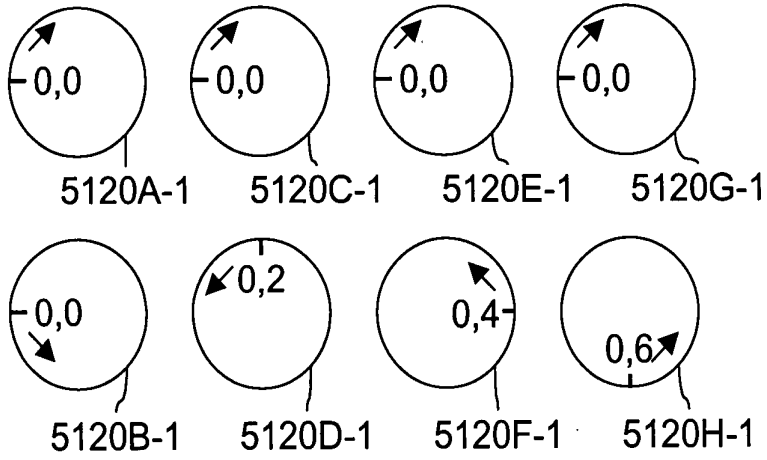


FIG. 51B

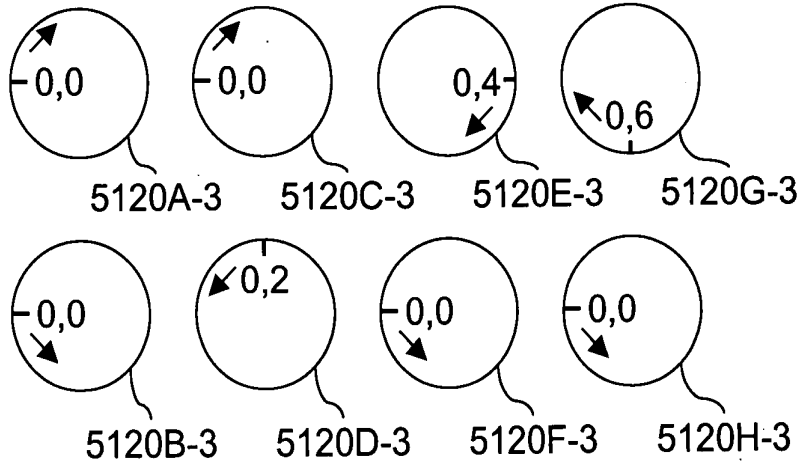


FIG. 51D

ROTATION PHASE t = 0 (T=8)

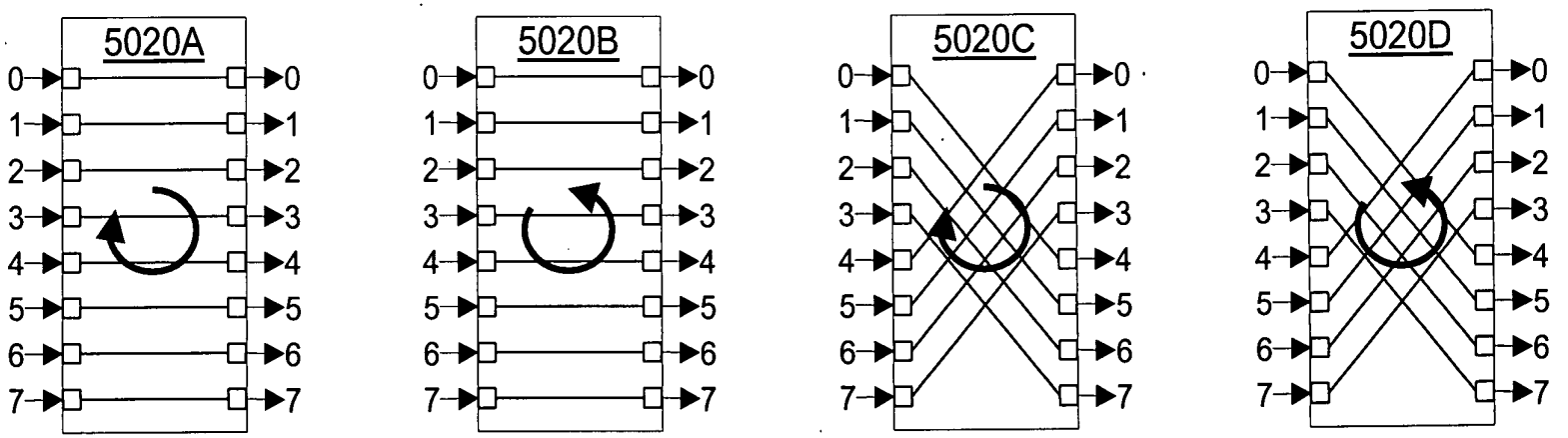


FIG. 52A

ROTATION PHASE t = 6 (T=8)

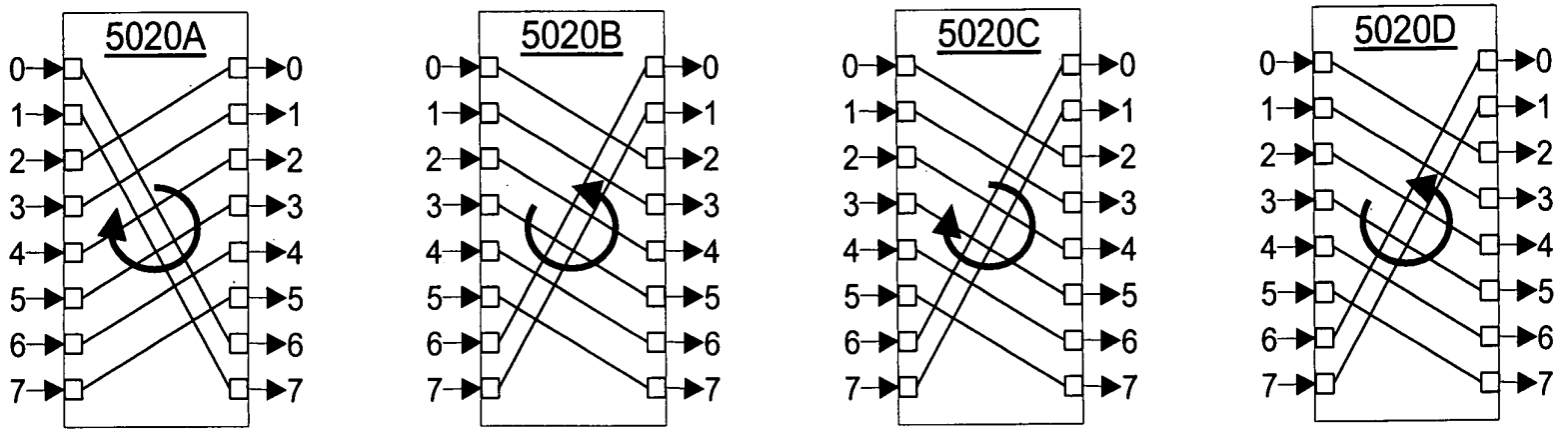


FIG. 52B

ROTATION PHASE t = 0 (T=7)

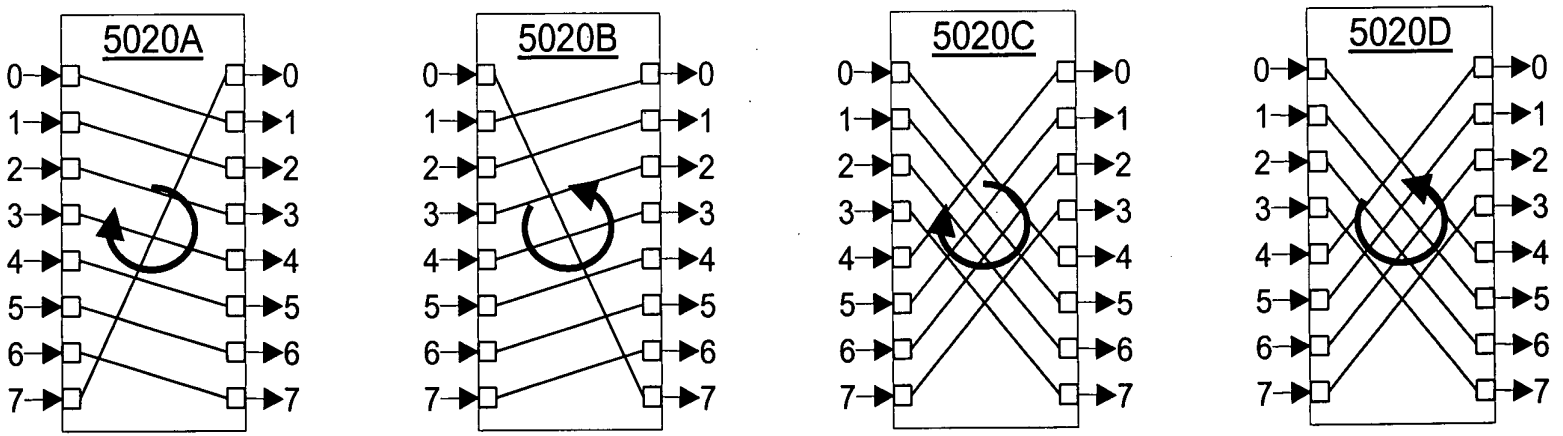


FIG. 53A

ROTATION PHASE t = 6 (T=7)

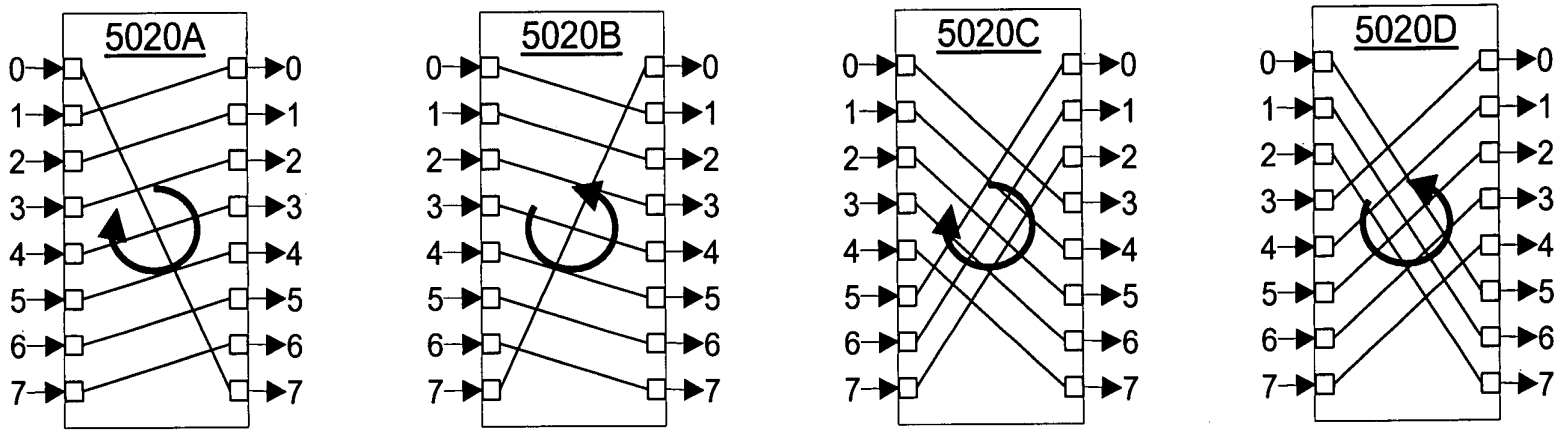


FIG. 53B

5400A

DESTINATION SWITCH MODULE →

SOURCE SWITCH MODULE ↓

	0	1	2	3	4	5	6	7
0	x	7	6	5	4	3	2	1
1	1	x	7	6	5	4	3	2
2	2	1	x	7	6	5	4	3
3	3	2	1	x	7	6	5	4
4	4	3	2	1	x	7	6	5
5	5	4	3	2	1	x	7	6
6	6	5	4	3	2	1	x	7
7	7	6	5	4	3	2	1	x

5460

5400B

DESTINATION SWITCH MODULE →

SOURCE SWITCH MODULE ↓

	0	1	2	3	4	5	6	7
0	x	1	2	3	4	5	6	7
1	7	x	1	2	3	4	5	6
2	6	7	x	1	2	3	4	5
3	5	6	7	x	1	2	3	4
4	4	5	6	7	x	1	2	3
5	3	4	5	6	7	x	1	2
6	2	3	4	5	6	7	x	1
7	1	2	3	4	5	6	7	x

5400C

DESTINATION SWITCH MODULE →

SOURCE SWITCH MODULE ↓

	0	1	2	3	4	5	6	7
0	x	3	2	1	8	7	6	5
1	5	x	3	2	1	8	7	5
2	6	5	x	3	2	1	8	7
3	7	6	5	x	3	2	1	8
4	8	7	6	5	x	3	2	1
5	1	8	7	6	5	x	3	2
6	2	1	8	7	6	5	x	3
7	3	2	1	8	7	6	5	x

5400D

DESTINATION SWITCH MODULE →

SOURCE SWITCH MODULE ↓

	0	1	2	3	4	5	6	7
0	x	5	6	7	8	1	2	3
1	3	x	5	6	7	8	1	2
2	2	3	x	5	6	7	8	1
3	1	2	3	x	5	6	7	8
4	8	1	2	3	x	5	6	7
5	7	8	1	2	3	x	5	6
6	6	7	8	1	2	3	x	5
7	5	6	7	8	1	2	3	x

5460

FIG. 54

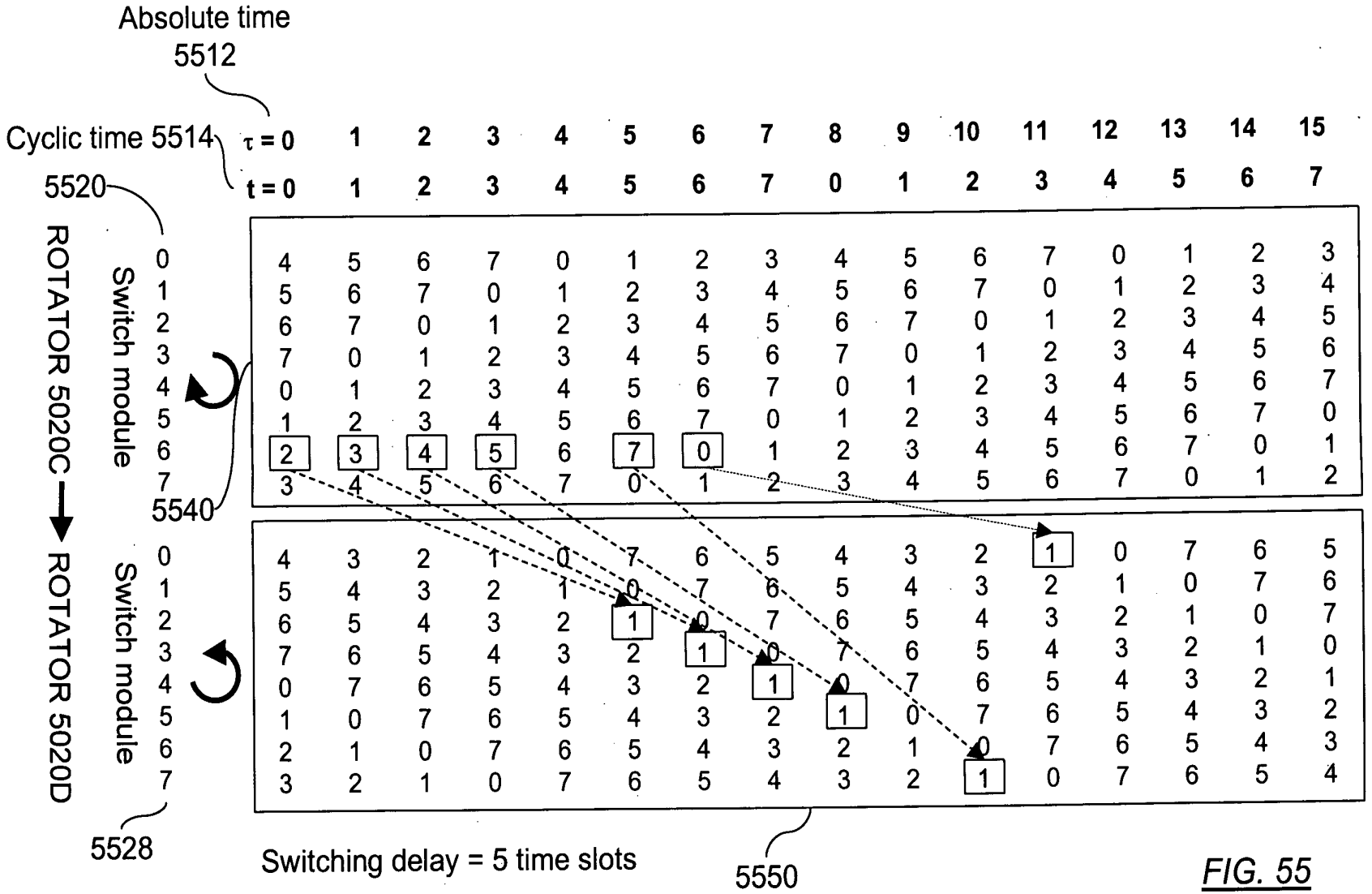

Absolute time
5512
Cyclic time 5514
5520
τ = 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
t = 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7
ROTATOR 5020C
ROTATOR 5020D
Switch module
Switch module
5540
5528
Switching delay = 5 time slots
5550

FIG. 55

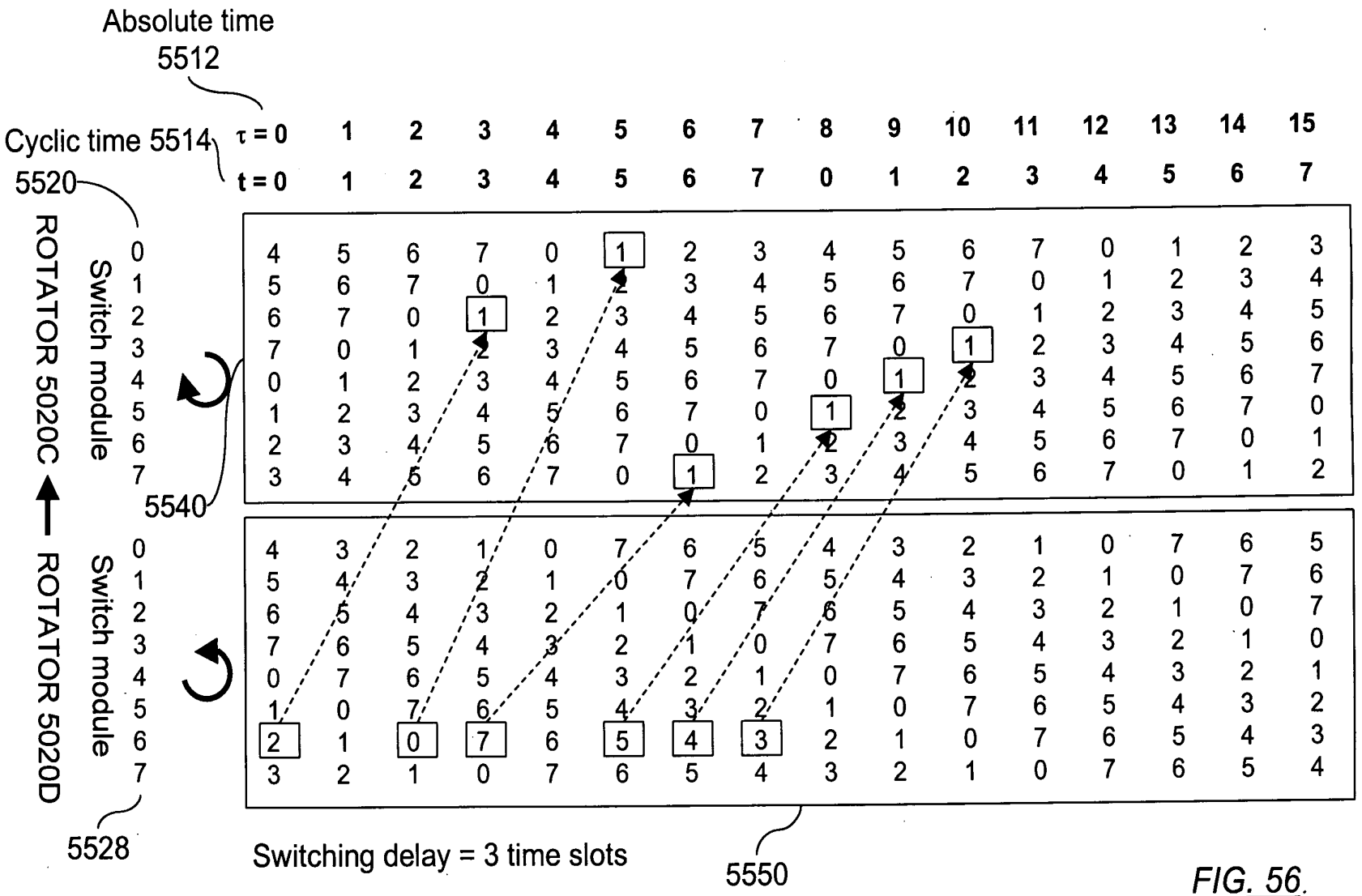

Absolute time
5512
Cyclic time 5514
5520
τ = 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
t = 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7
ROTATOR 5020C
ROTATOR 5020D
Switch module
Switch module
0 1 2 3 4 5 6 7
5540
5528
Switching delay = 3 time slots
5550

FIG. 56

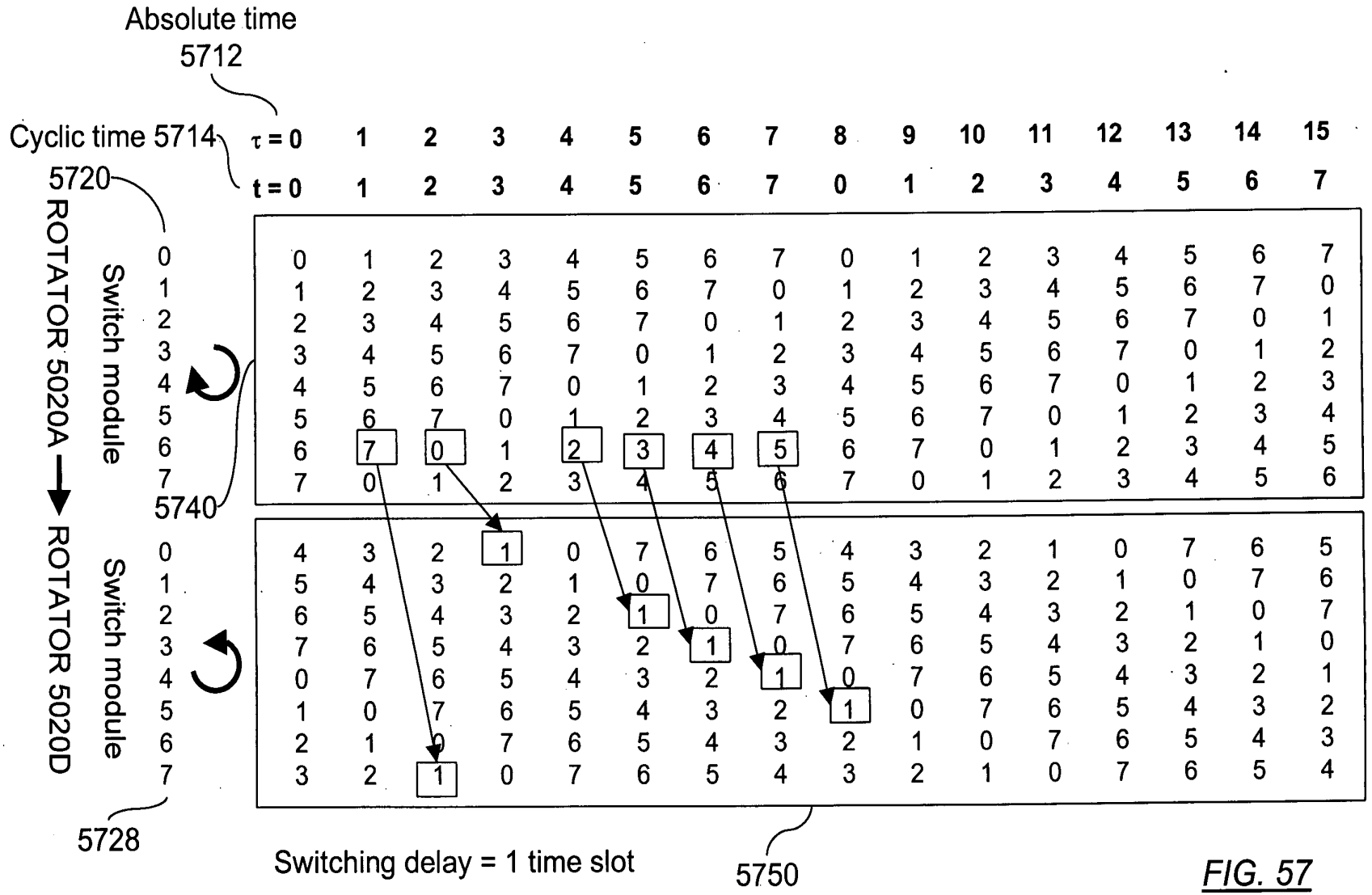

Absolute time
5712
Cyclic time 5714
5720
τ = 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
t = 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7
ROTATOR 5020A
Switch module
ROTATOR 5020D
Switch module
5740
5728
Switching delay = 1 time slot
5750

FIG. 57

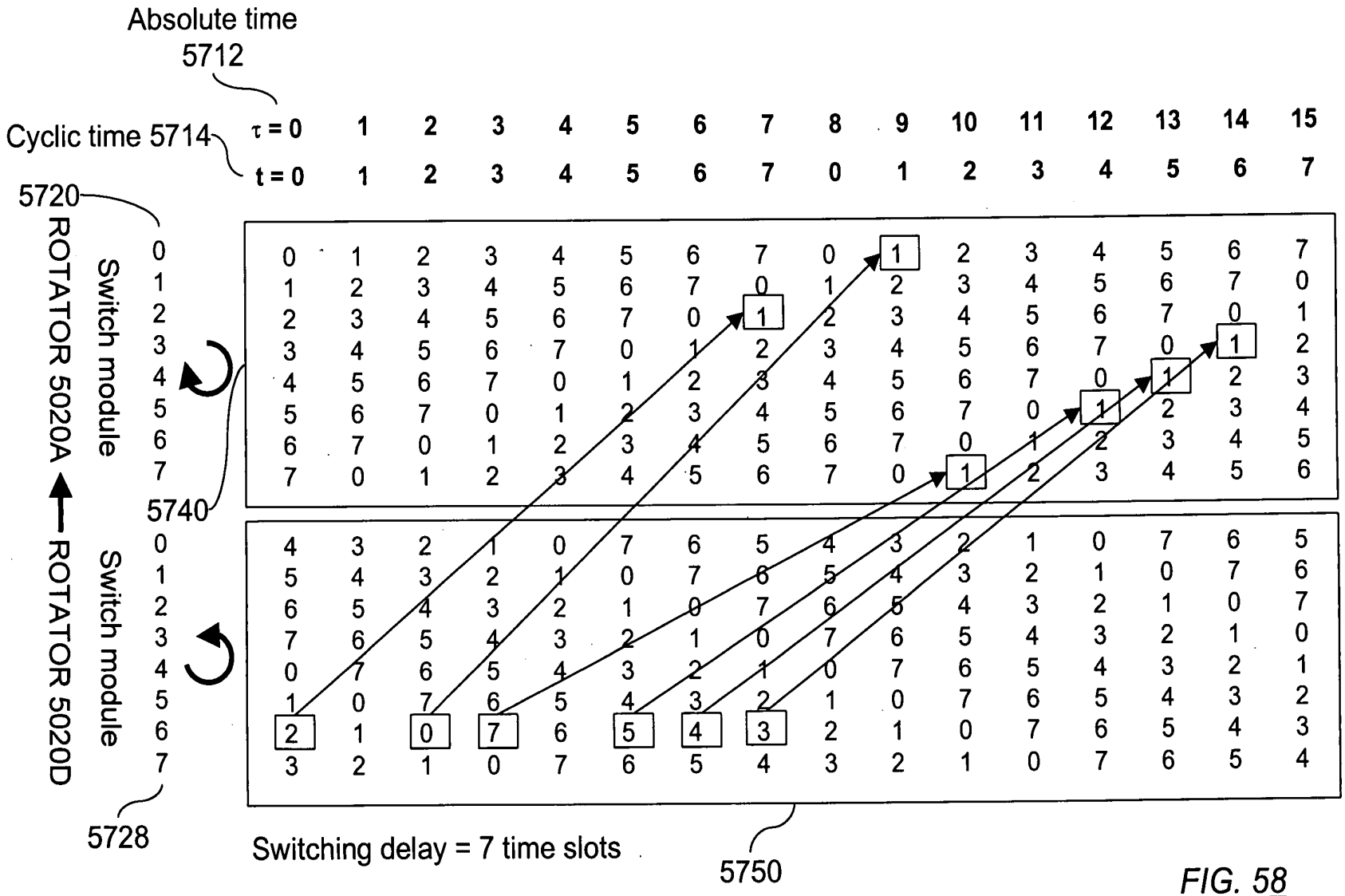

Absolute time
5712
Cyclic time 5714
τ = 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
t = 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7
5720
ROTATOR 5020A
Switch module
ROTATOR 5020D
Switch module
5740
5728
Switching delay = 7 time slots
5750

FIG. 58

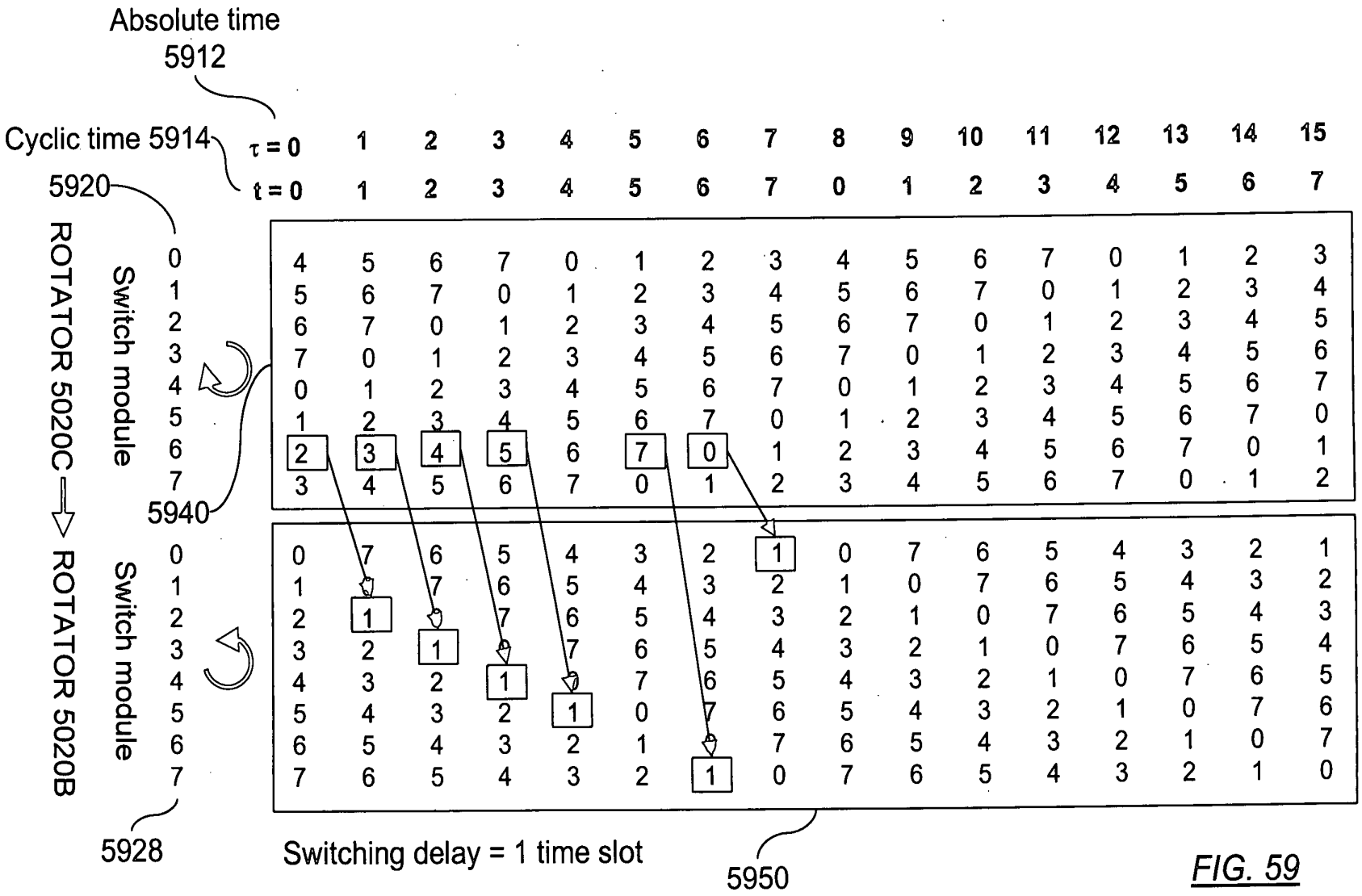

Absolute time
5912
Cyclic time 5914
τ = 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
t = 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7
5920
ROTATOR 5020C
ROTATOR 5020B
Switch module
Switch module
5940
5928
Switching delay = 1 time slot
5950

FIG. 59

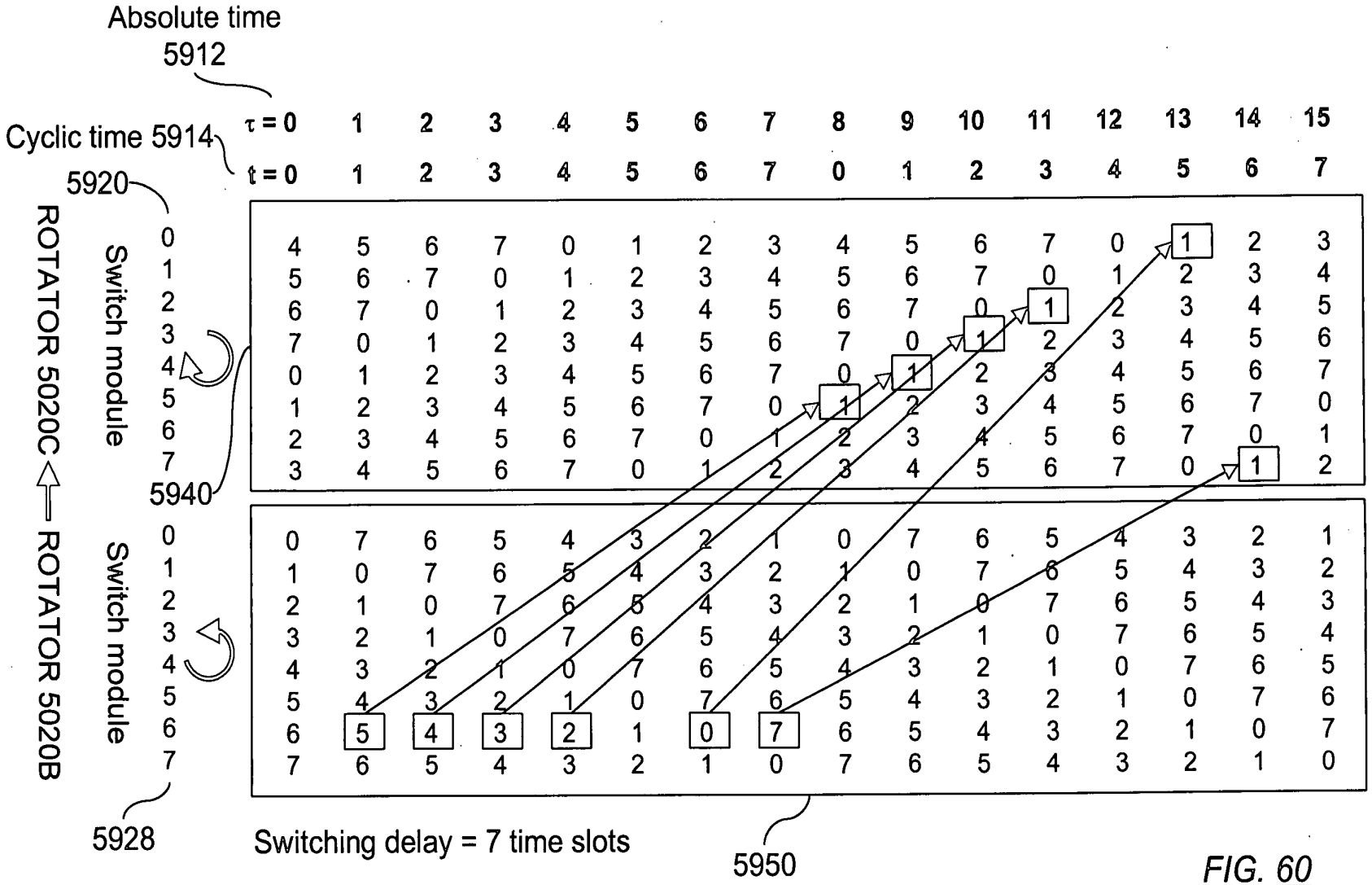

Absolute time
5912
Cyclic time 5914
5920
τ = 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
t = 0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7
Switch module
5940
Switch module
5928
ROTATOR 5020C
ROTATOR 5020B
Switching delay = 7 time slots
5950

FIG. 60

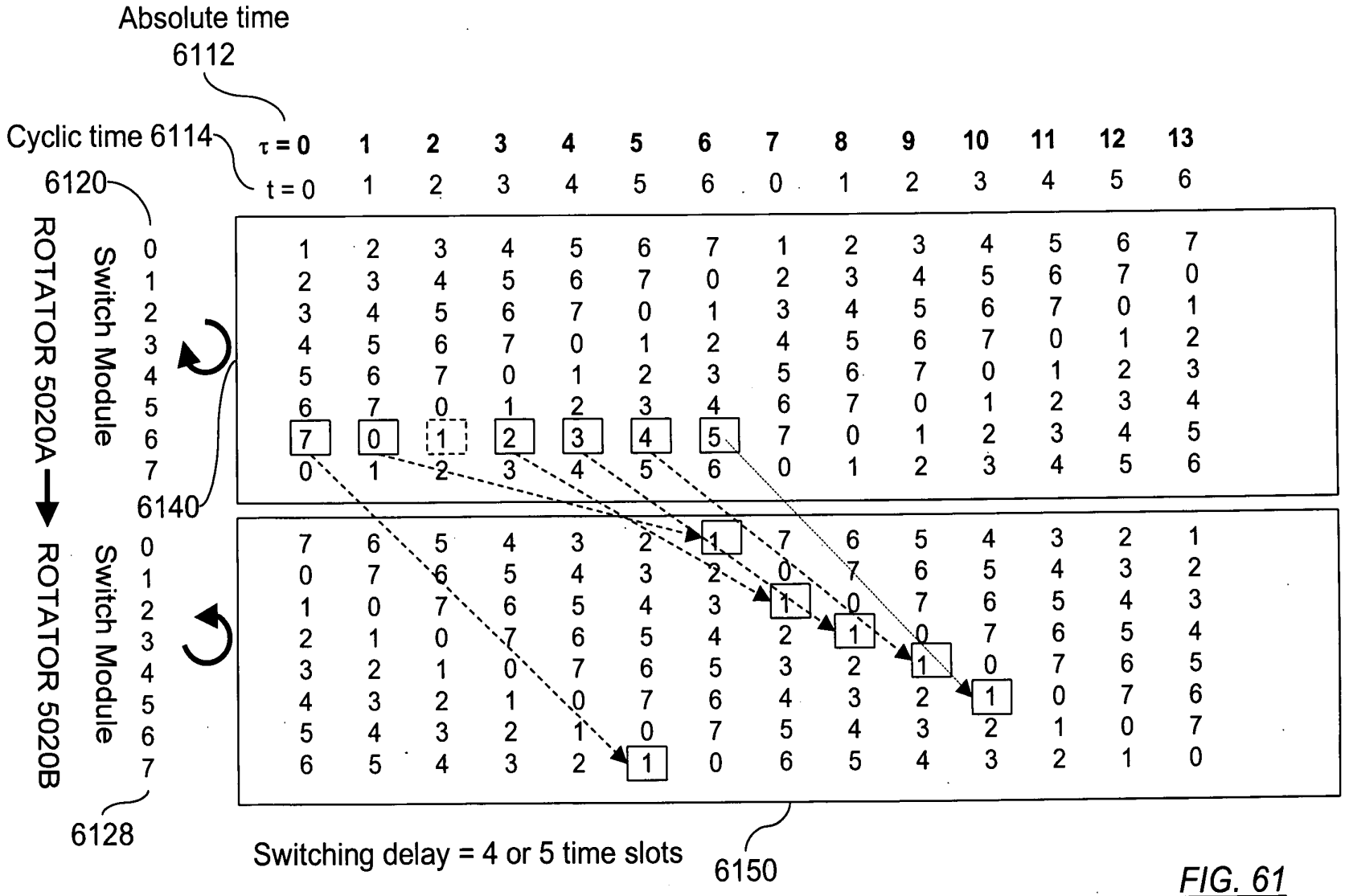

Absolute time
6112
Cyclic time 6114
6120
τ = 0 1 2 3 4 5 6 7 8 9 10 11 12 13
t = 0 1 2 3 4 5 6 0 1 2 3 4 5 6
ROTATOR 5020A
Switch Module
0 1 2 3 4 5 6 7
6140
1 2 3 4 5 6 7 1 2 3 4 5 6 7
2 3 4 5 6 7 0 2 3 4 5 6 7 0
3 4 5 6 7 0 1 3 4 5 6 7 0 1
4 5 6 7 0 1 2 4 5 6 7 0 1 2
5 6 7 0 1 2 3 5 6 7 0 1 2 3
6 7 0 1 2 3 4 6 7 0 1 2 3 4
7 0 1 2 3 4 5 7 0 1 2 3 4 5
0 1 2 3 4 5 6 0 1 2 3 4 5 6
ROTATOR 5020B
Switch Module
0 1 2 3 4 5 6 7
6128
7 6 5 4 3 2 1 7 6 5 4 3 2 1
0 7 6 5 4 3 2 0 7 6 5 4 3 2
1 0 7 6 5 4 3 1 0 7 6 5 4 3
2 1 0 7 6 5 4 2 1 0 7 6 5 4
3 2 1 0 7 6 5 3 2 1 0 7 6 5
4 3 2 1 0 7 6 4 3 2 1 0 7 6
5 4 3 2 1 0 7 5 4 3 2 1 0 7
6 5 4 3 2 1 0 6 5 4 3 2 1 0
Switching delay = 4 or 5 time slots
6150

FIG. 61

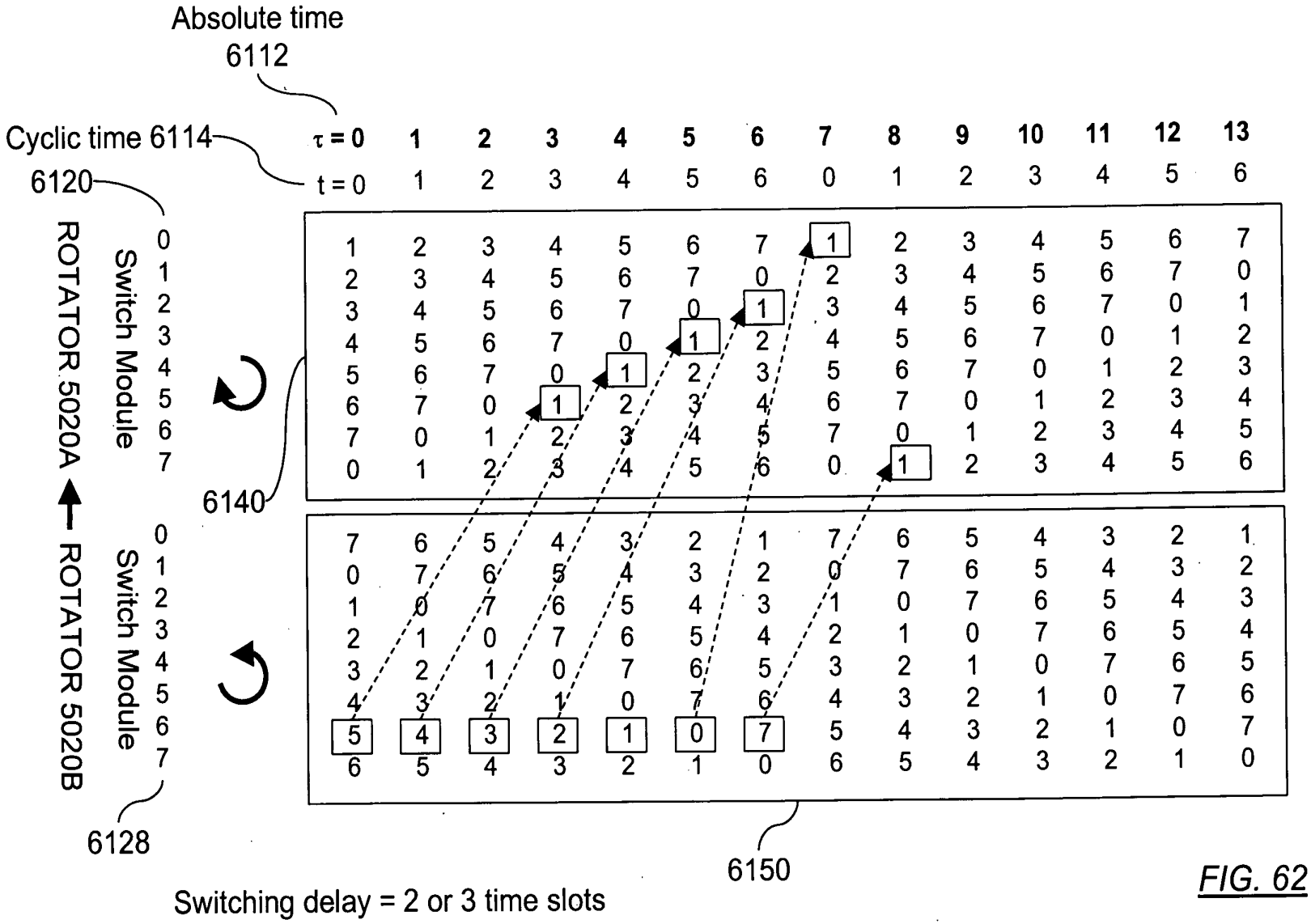

Absolute time
6112
Cyclic time 6114
6120
τ = 0 1 2 3 4 5 6 7 8 9 10 11 12 13
t = 0 1 2 3 4 5 6 0 1 2 3 4 5 6
Switch Module
ROTATOR 5020A
ROTATOR 5020B
Switch Module
6140
6128
6150
Switching delay = 2 or 3 time slots

FIG. 62

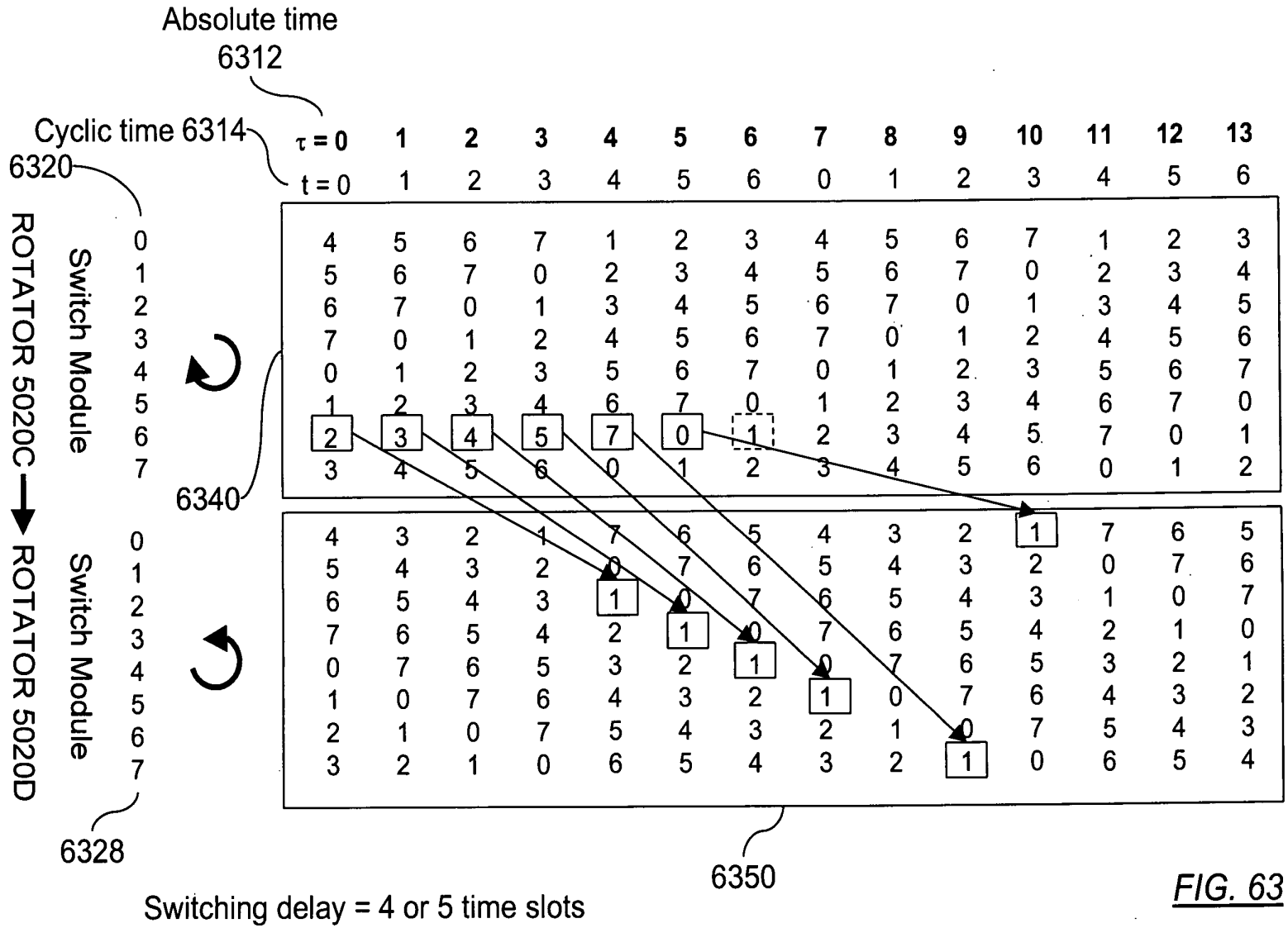

Absolute time
6312
Cyclic time 6314
6320
τ = 0 1 2 3 4 5 6 7 8 9 10 11 12 13
t = 0 1 2 3 4 5 6 0 1 2 3 4 5 6
ROTATOR 5020C
ROTATOR 5020D
Switch Module
Switch Module
0 1 2 3 4 5 6 7
6340
6328
6350
Switching delay = 4 or 5 time slots

FIG. 63

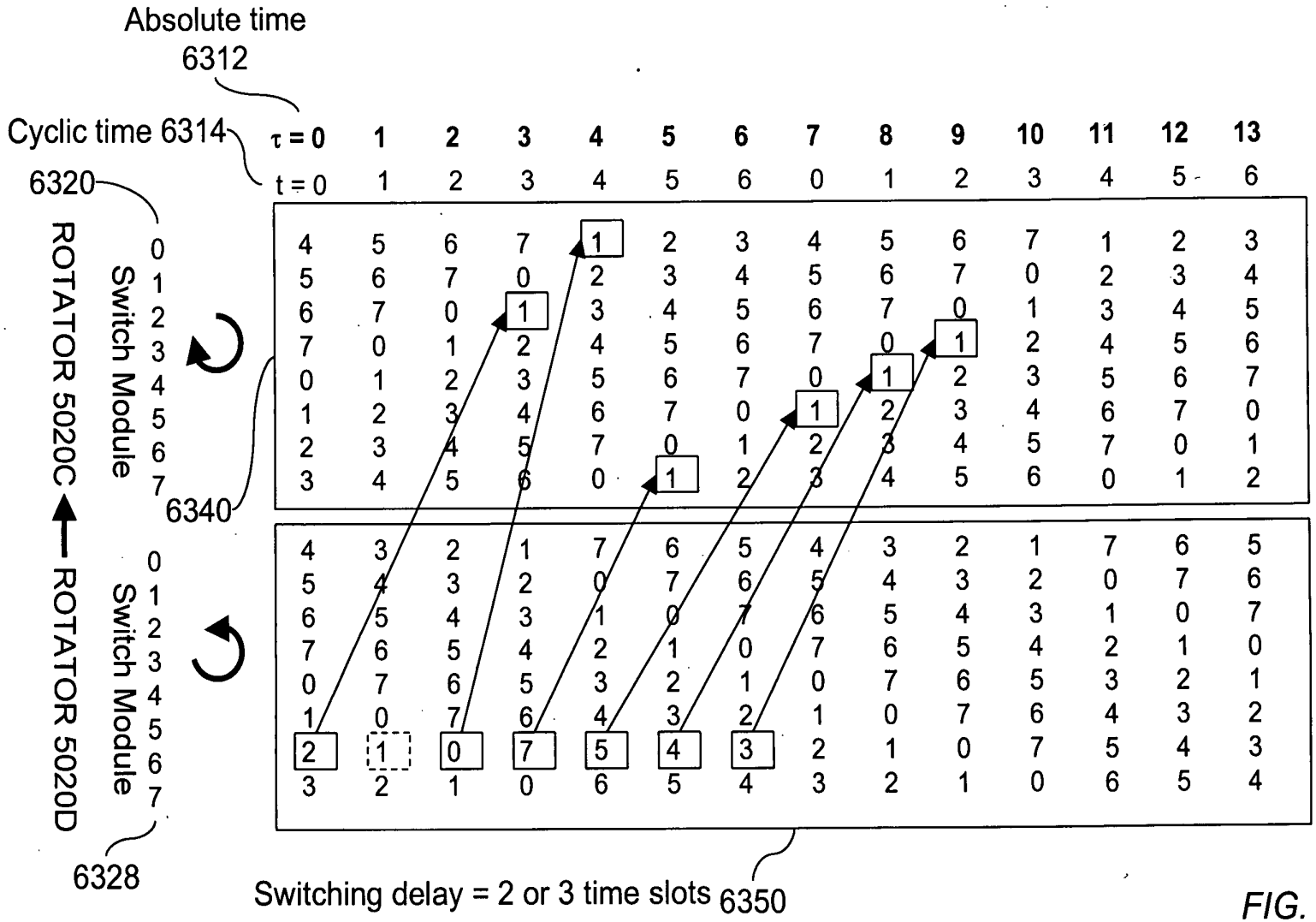
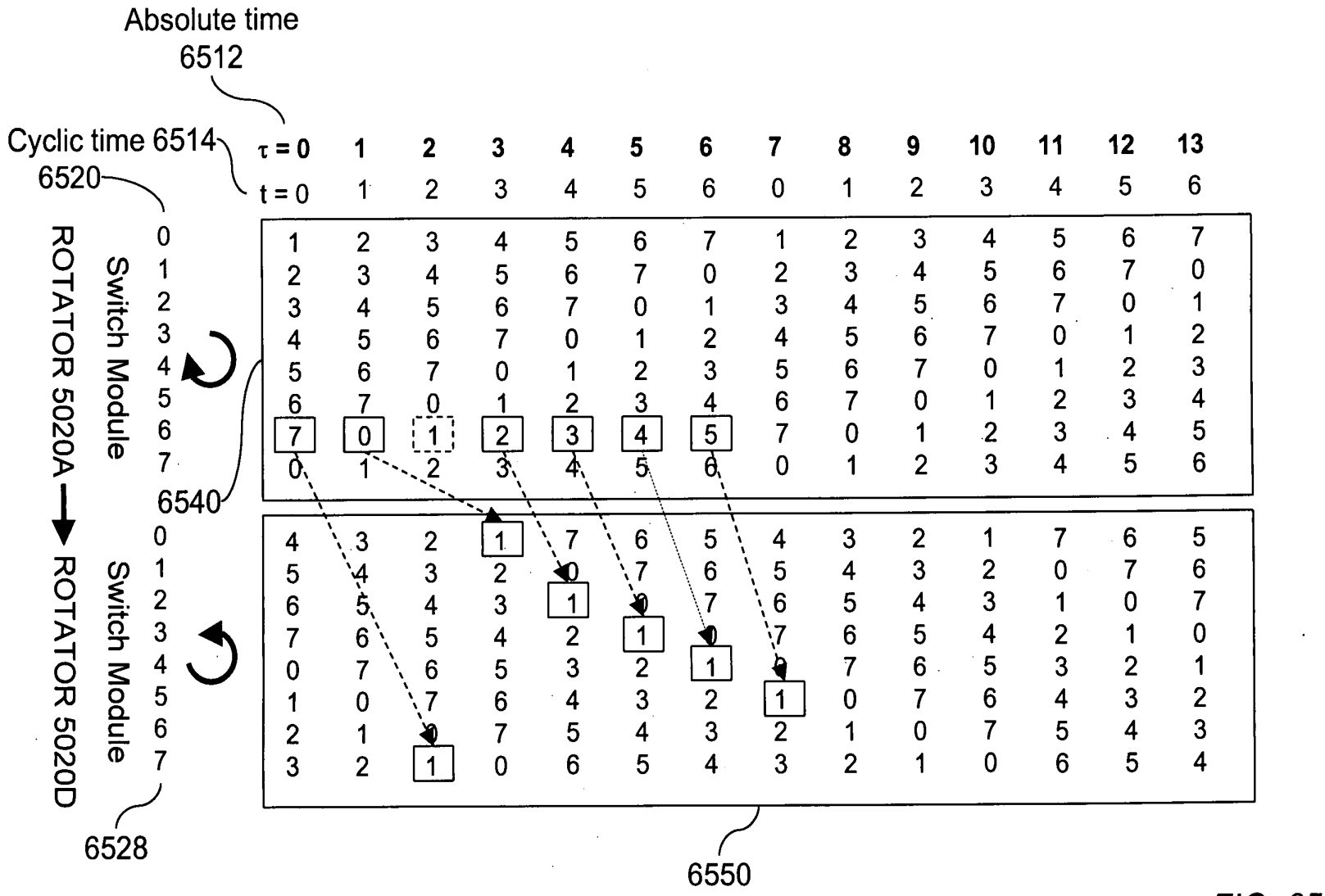

Absolute time
6312
Cyclic time 6314
6320
τ = 0 1 2 3 4 5 6 7 8 9 10 11 12 13
t = 0 1 2 3 4 5 6 0 1 2 3 4 5 6
ROTATOR 5020C
Switch Module
0 1 2 3 4 5 6 7
6340
ROTATOR 5020D
Switch Module
0 1 2 3 4 5 6 7
6328
Switching delay = 2 or 3 time slots
6350

FIG. 64



Switching delay = 1 time slot or 2 time slots

FIG. 65

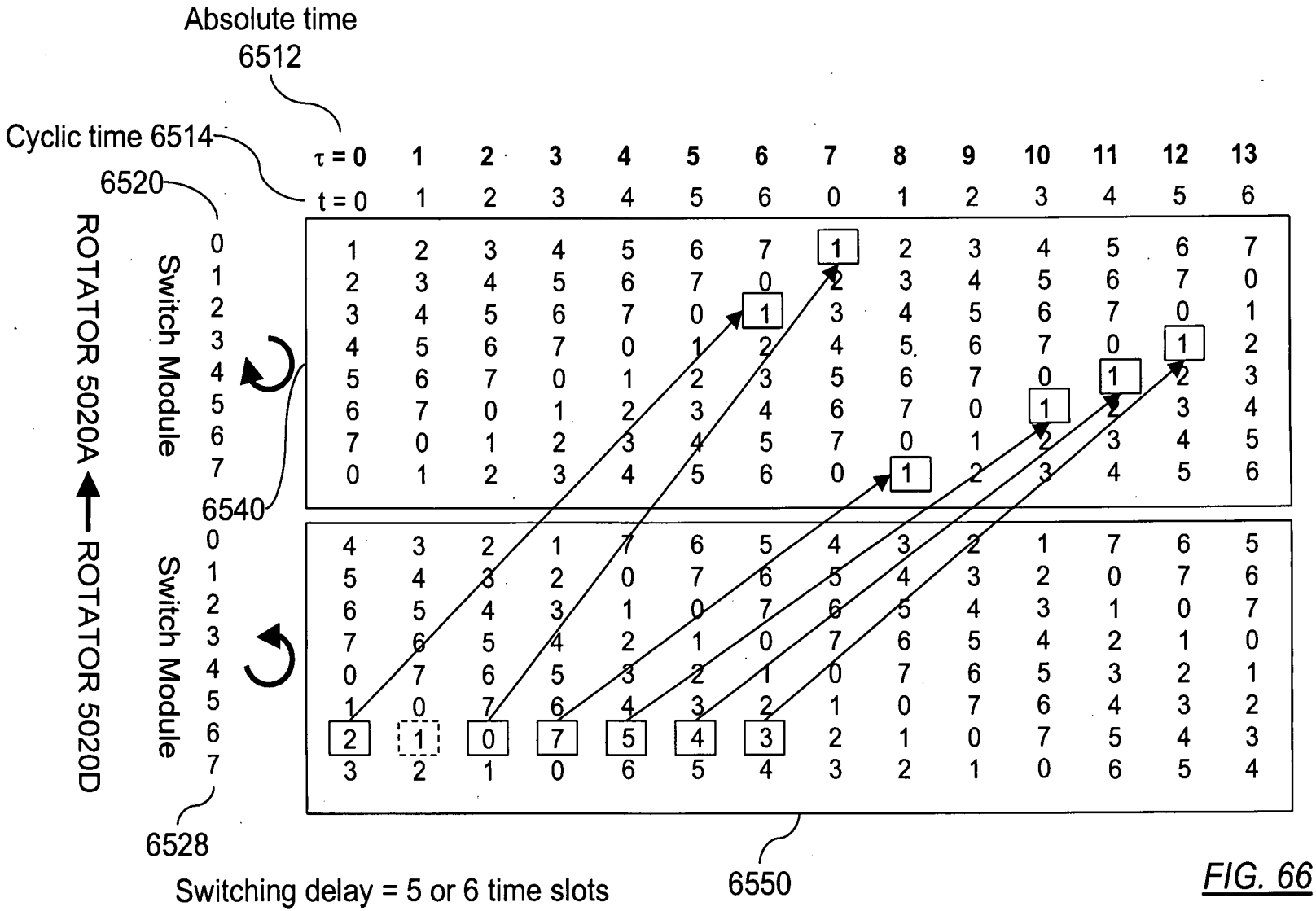

Absolute time
6512
Cyclic time 6514
6520
τ = 0 1 2 3 4 5 6 7 8 9 10 11 12 13
t = 0 1 2 3 4 5 6 0 1 2 3 4 5 6
Switch Module
Switch Module
ROTATOR 5020A
ROTATOR 5020D
6540
6528
6550
Switching delay = 5 or 6 time slots

FIG. 66

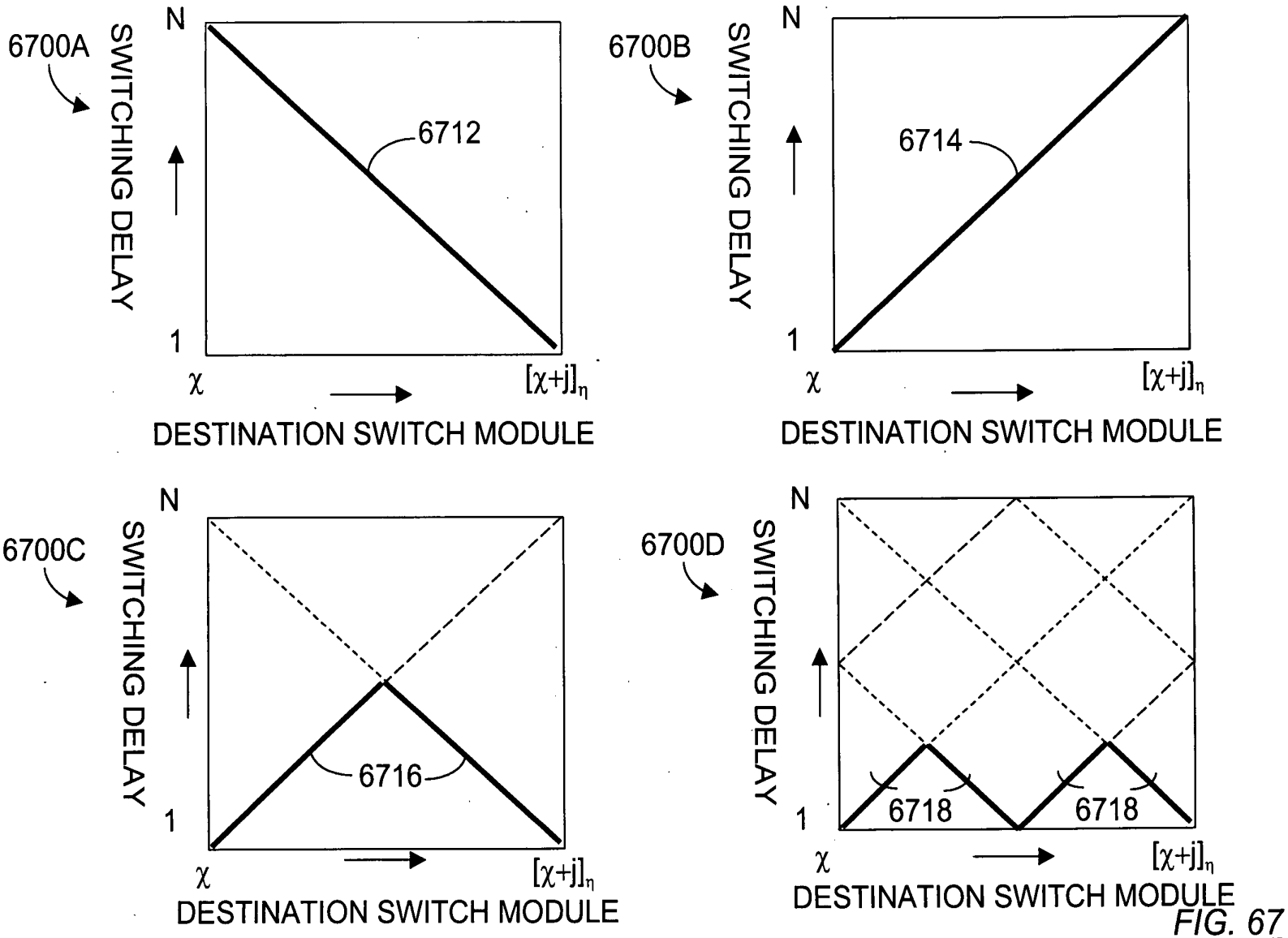

6700A
N
SWITCHING DELAY
6712
1
χ
[χ+j]η
DESTINATION SWITCH MODULE
6700B
N
SWITCHING DELAY
6714
1
χ
[χ+j]η
DESTINATION SWITCH MODULE
6700C
N
SWITCHING DELAY
6716
1
χ
[χ+j]η
DESTINATION SWITCH MODULE
6700D
N
SWITCHING DELAY
6718
6718
1
χ
[χ+j]η
DESTINATION SWITCH MODULE

FIG. 67

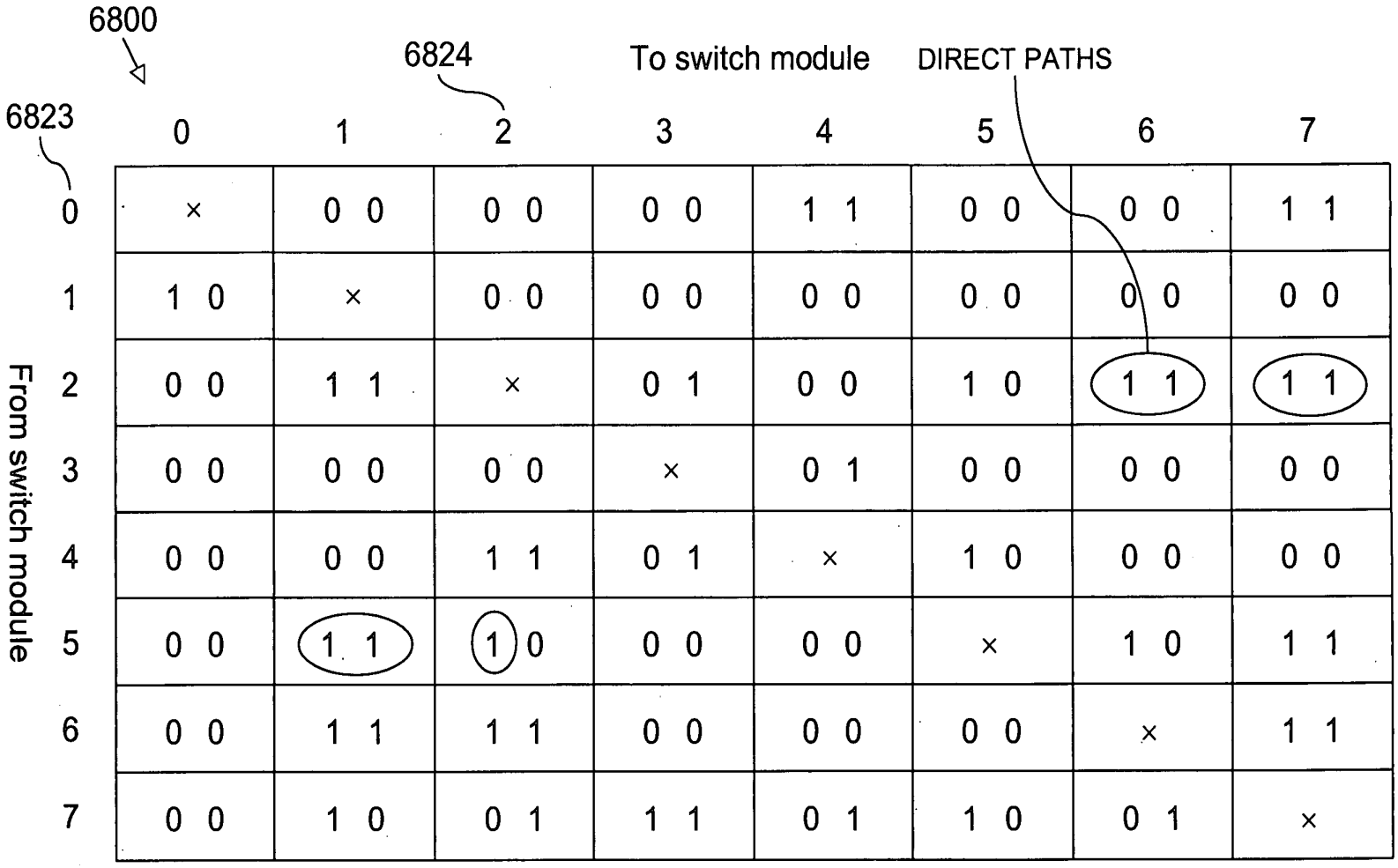

6800
6824
To switch module
DIRECT PATHS
6823
From switch module
0 1 2 3 4 5 6 7
0 × 0 0 0 0 0 0 1 1 0 0 0 0
1 1 0 × 0 0 0 0 0 0 0 0 0 0
2 0 0 1 1 × 0 1 0 0 1 0 1 1 1 1
3 0 0 0 0 0 0 × 0 1 0 0 0 0
4 0 0 0 0 1 1 0 1 × 1 0 0 0
5 0 0 1 1 1 0 0 0 0 0 × 1 0 1 1
6 0 0 1 1 1 1 0 0 0 0 0 0 × 1 1
7 0 0 1 0 0 1 1 1 0 1 1 0 0 1 ×

FIG. 68

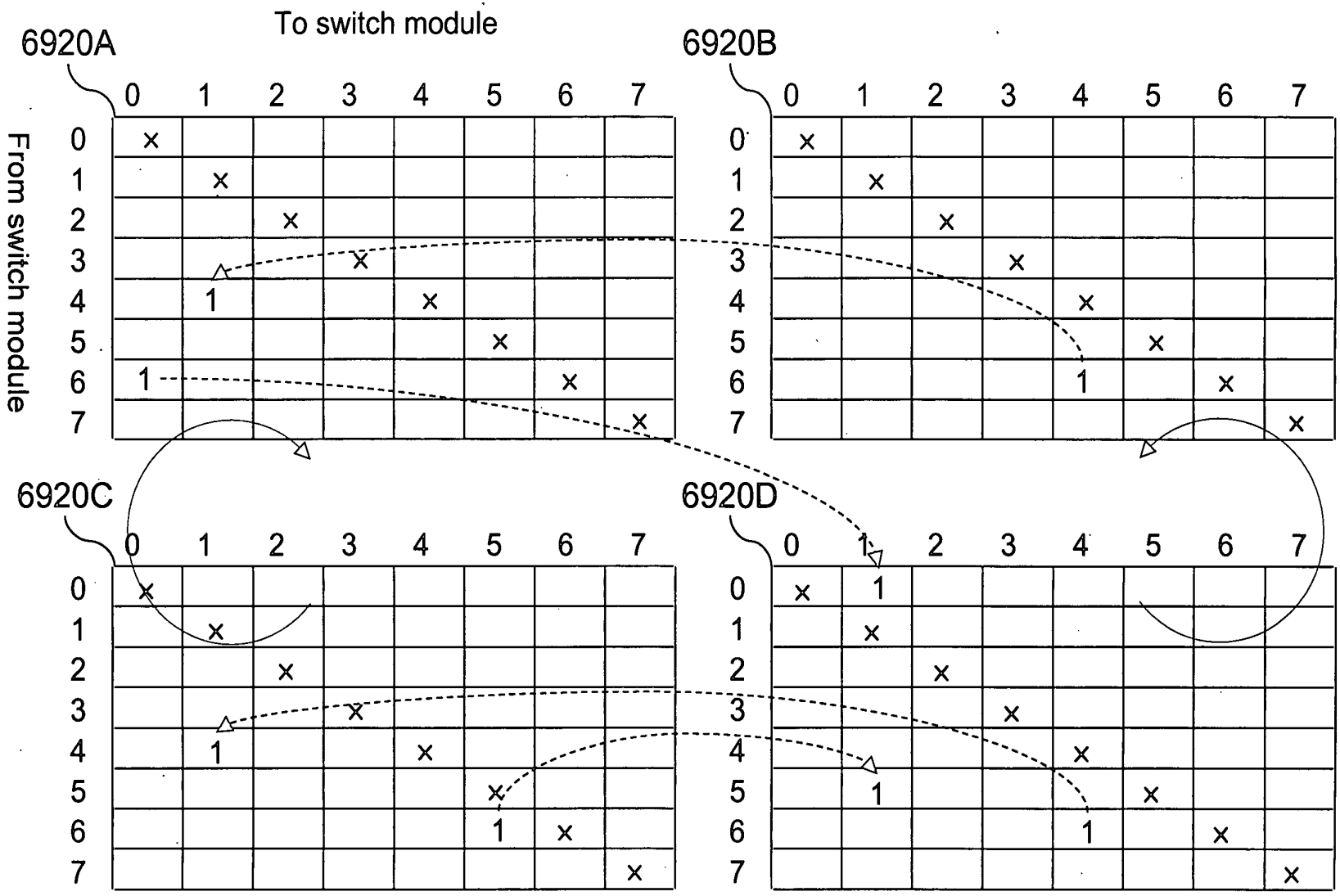

6920A
To switch module
From switch module
0 1 2 3 4 5 6 7
0 ×
1 ×
2 ×
3 × 1
4 1 ×
5 ×
6 1 ×
7 ×
6920B
0 1 2 3 4 5 6 7
0 ×
1 ×
2 ×
3 ×
4 ×
5 ×
6 1 ×
7 ×
6920C
0 1 2 3 4 5 6 7
0 ×
1 ×
2 ×
3 ×
4 1 ×
5 ×
6 1 ×
7 ×
6920D
0 1 2 3 4 5 6 7
0 × 1
1 ×
2 ×
3 ×
4 ×
5 1 ×
6 1 ×
7 ×

FIG. 69

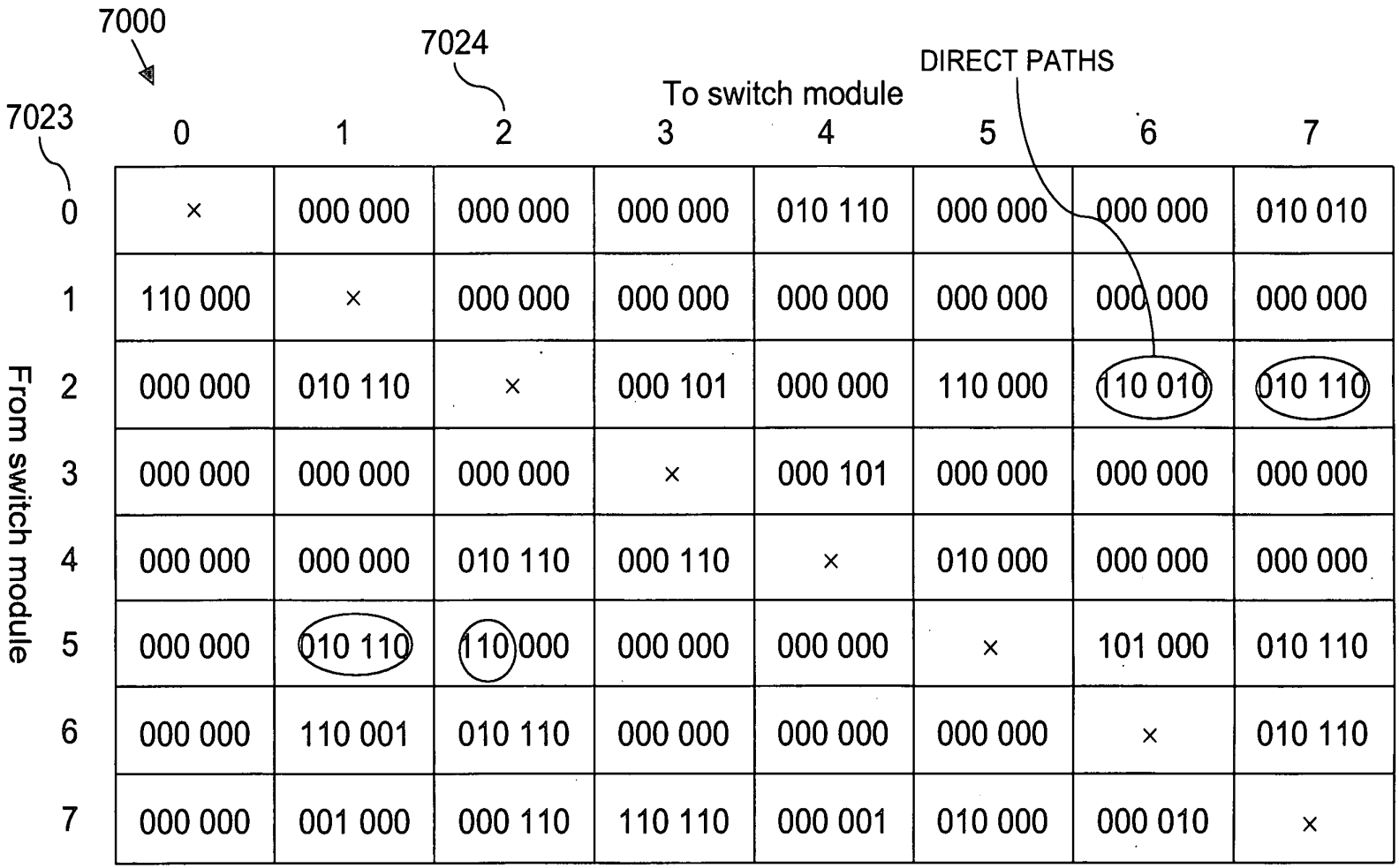

7000
7024
DIRECT PATHS
To switch module
7023
0 1 2 3 4 5 6 7
From switch module
0 × 000 000 000 000 010 110 000 000 000 000 010 010
1 110 000 × 000 000 000 000 000 000 000 000 000 000
2 000 000 010 110 × 000 101 000 000 110 000 110 010 010 110
3 000 000 000 000 000 000 × 000 101 000 000 000 000 000 000
4 000 000 000 000 010 110 000 110 × 010 000 000 000 000 000
5 000 000 010 110 110 000 000 000 000 000 × 101 000 010 110
6 000 000 110 001 010 110 000 000 000 000 000 000 × 010 110
7 000 000 001 000 000 110 110 110 000 001 010 000 000 010 ×

FIG. 70

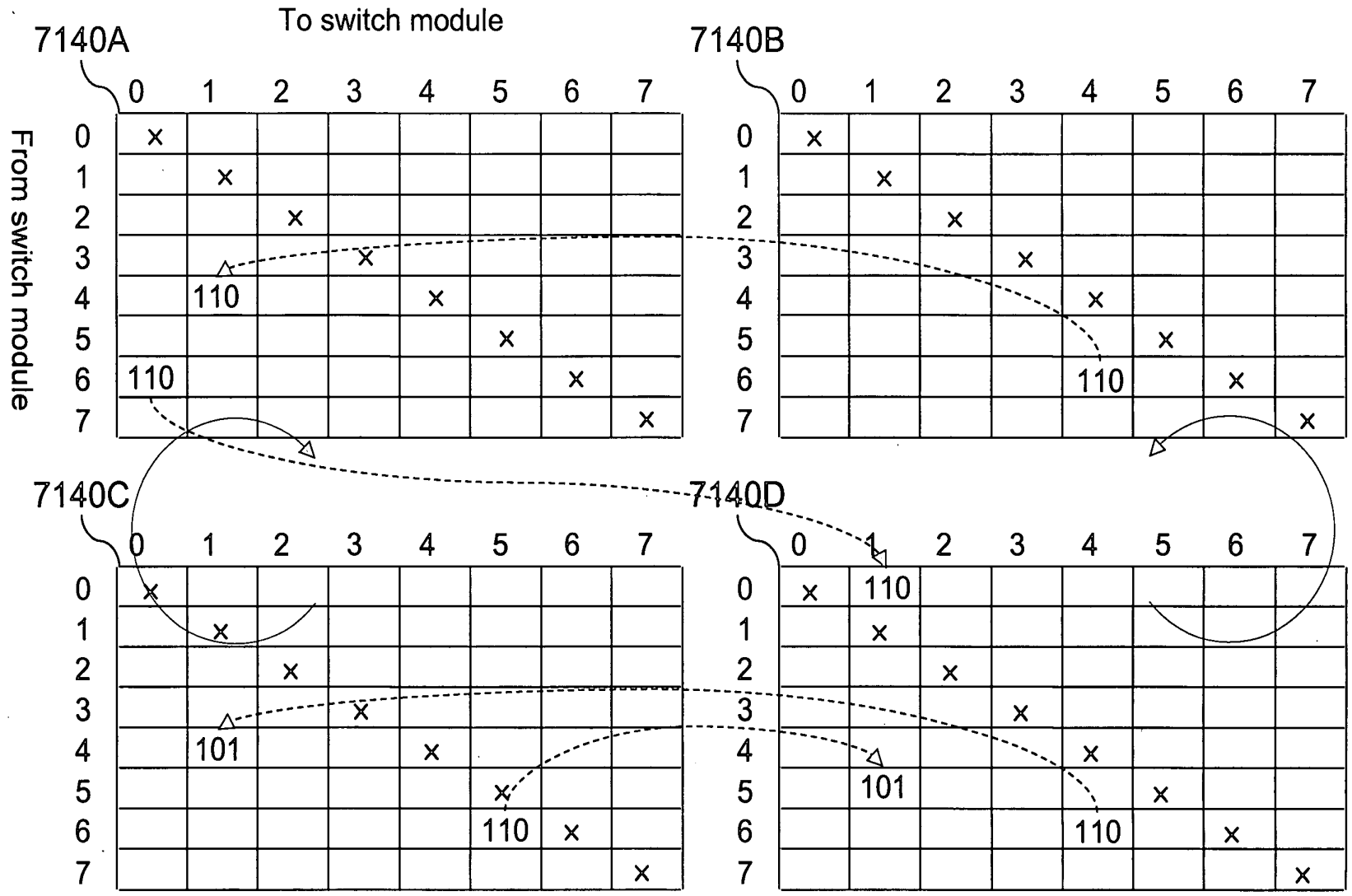

To switch module
From switch module
7140A
7140B
7140C
7140D
0 1 2 3 4 5 6 7
110
101

FIG. 71

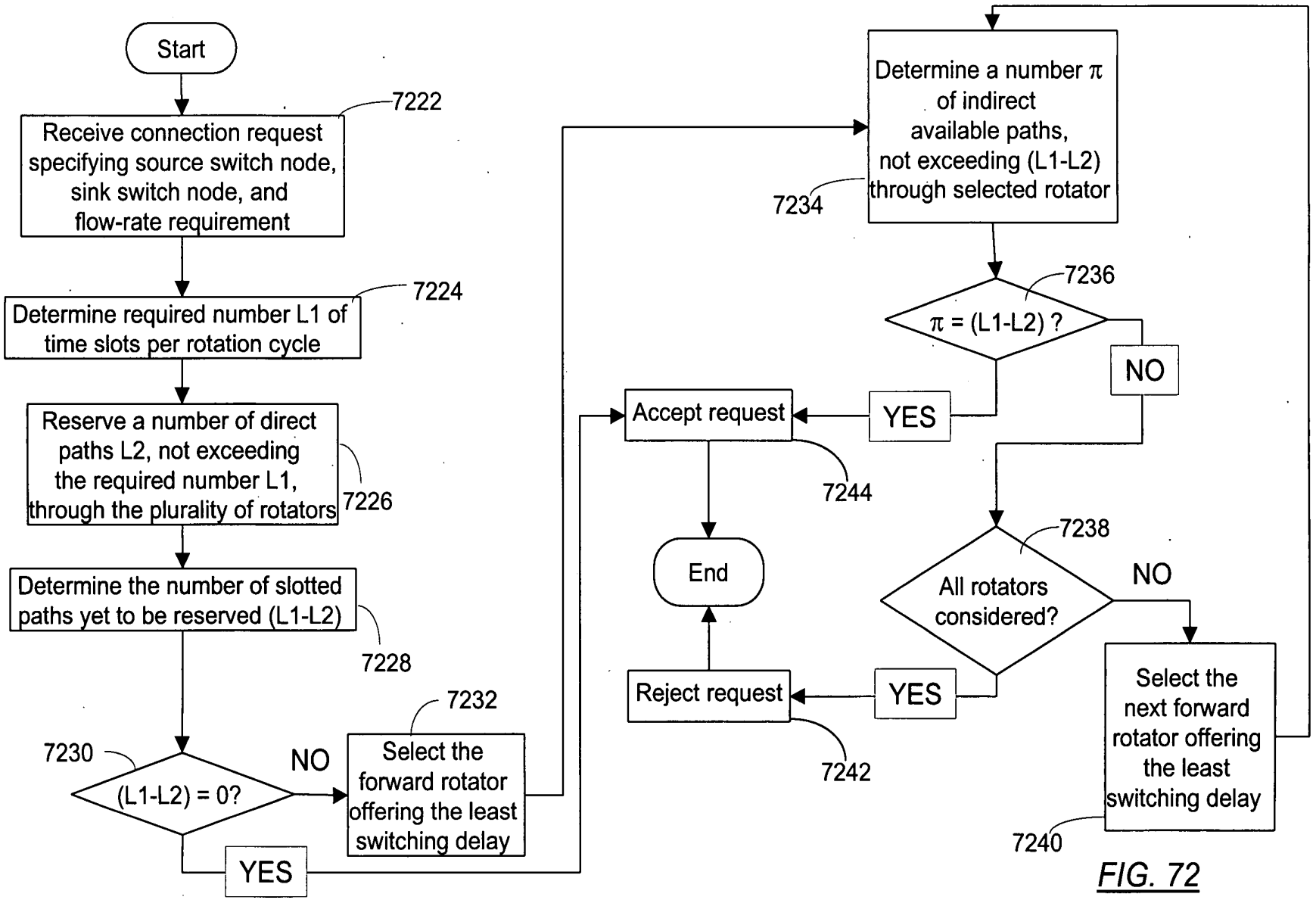

Start
Receive connection request specifying source switch node, sink switch node, and flow-rate requirement
7222
Determine required number L1 of time slots per rotation cycle
7224
Reserve a number of direct paths L2, not exceeding the required number L1, through the plurality of rotators
7226
Determine the number of slotted paths yet to be reserved (L1-L2)
7228
7230
(L1-L2) = 0?
NO
7232
Select the forward rotator offering the least switching delay
YES
Determine a number π of indirect available paths, not exceeding (L1-L2) through selected rotator
7234
7236
π = (L1-L2) ?
NO
YES
Accept request
7244
End
7238
All rotators considered?
NO
YES
Reject request
7242
Select the next forward rotator offering the least switching delay
7240

FIG. 72

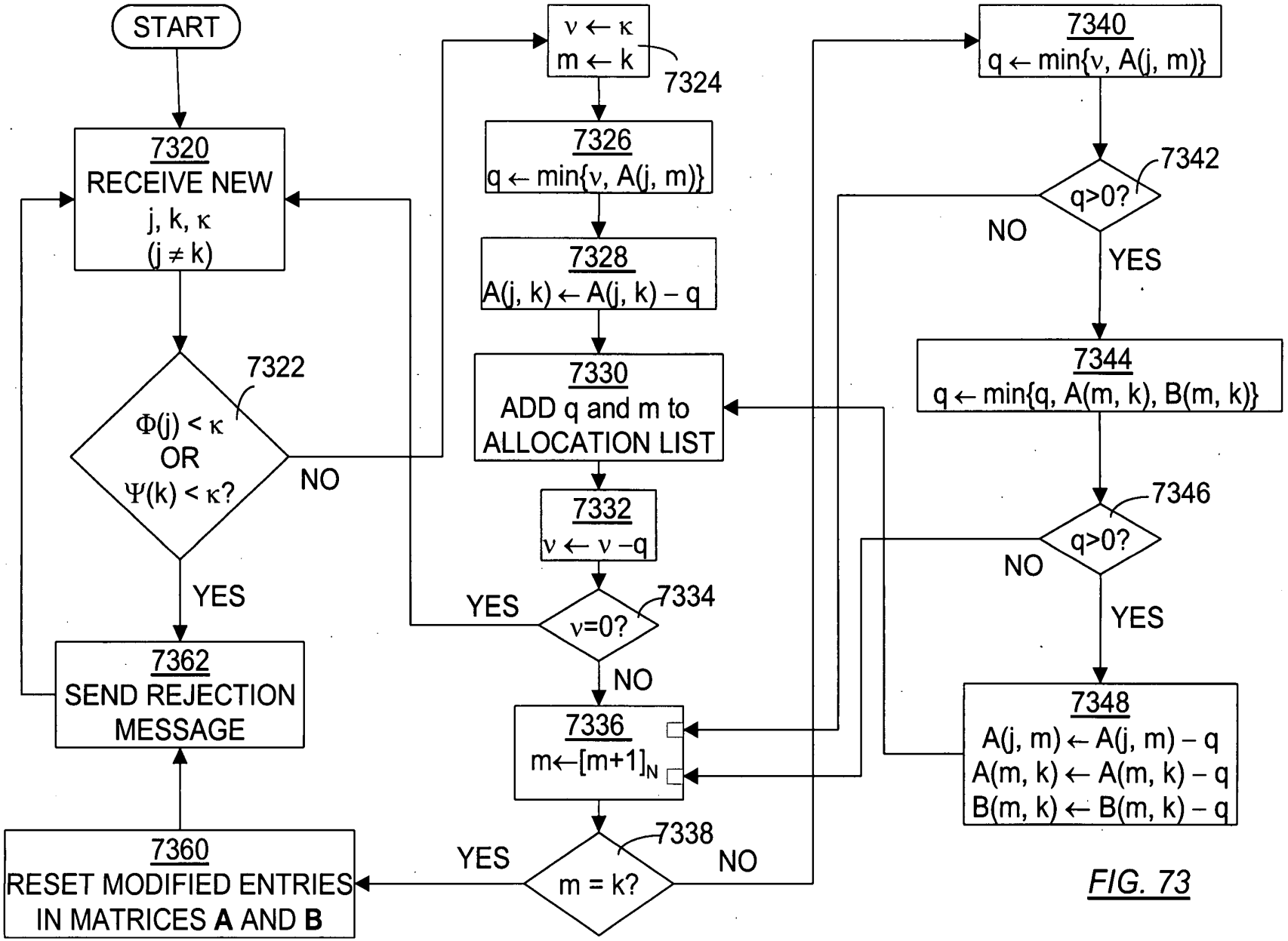

START
7320
RECEIVE NEW
j, k, κ
(j ≠ k)
7322
Φ(j) < κ
OR
Ψ(k) < κ?
NO
YES
7362
SEND REJECTION
MESSAGE
7360
RESET MODIFIED ENTRIES
IN MATRICES A AND B
ν ← κ
m ← k
7324
7326
q ← min{ν, A(j, m)}
7328
A(j, k) ← A(j, k) – q
7330
ADD q and m to
ALLOCATION LIST
7332
ν ← ν –q
7334
ν=0?
YES
NO
7336
m←[m+1]N
7338
m = k?
YES
NO
7340
q ← min{ν, A(j, m)}
7342
q>0?
NO
YES
7344
q ← min{q, A(m, k), B(m, k)}
7346
q>0?
NO
YES
7348
A(j, m) ← A(j, m) – q
A(m, k) ← A(m, k) – q
B(m, k) ← B(m, k) – q

FIG. 73

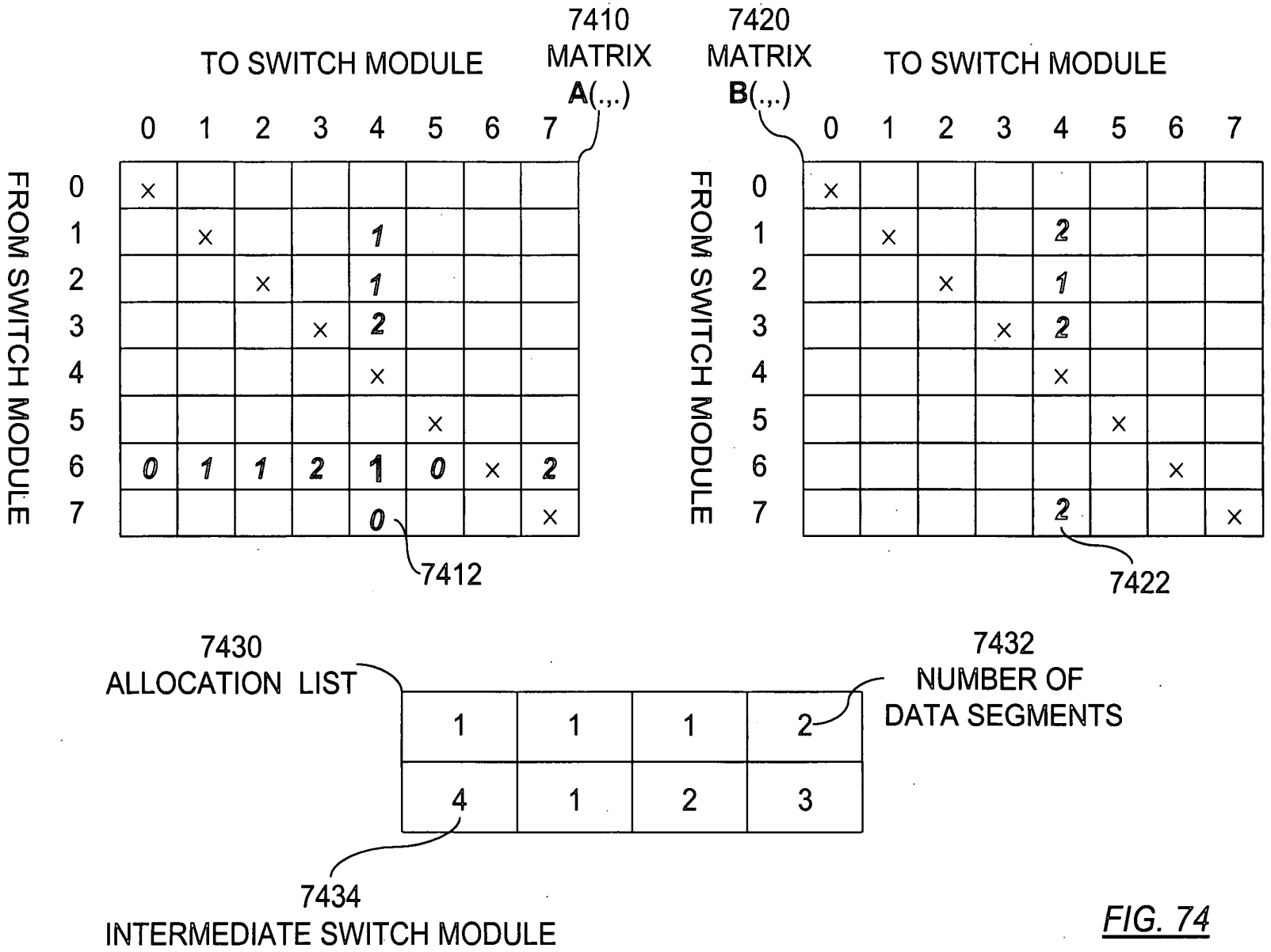

7410
MATRIX
A(.,.)
TO SWITCH MODULE
FROM SWITCH MODULE
0 1 2 3 4 5 6 7
0 ×
1 × 1
2 × 1
3 × 2
4 ×
5 ×
6 0 1 1 2 1 0 × 2
7 0 ×
7412
7420
MATRIX
B(.,.)
TO SWITCH MODULE
FROM SWITCH MODULE
0 1 2 3 4 5 6 7
0 ×
1 × 2
2 × 1
3 × 2
4 ×
5 ×
6 ×
7 2 ×
7422
7430
ALLOCATION LIST
7432
NUMBER OF
DATA SEGMENTS
1 1 1 2
4 1 2 3
7434
INTERMEDIATE SWITCH MODULE

FIG. 74

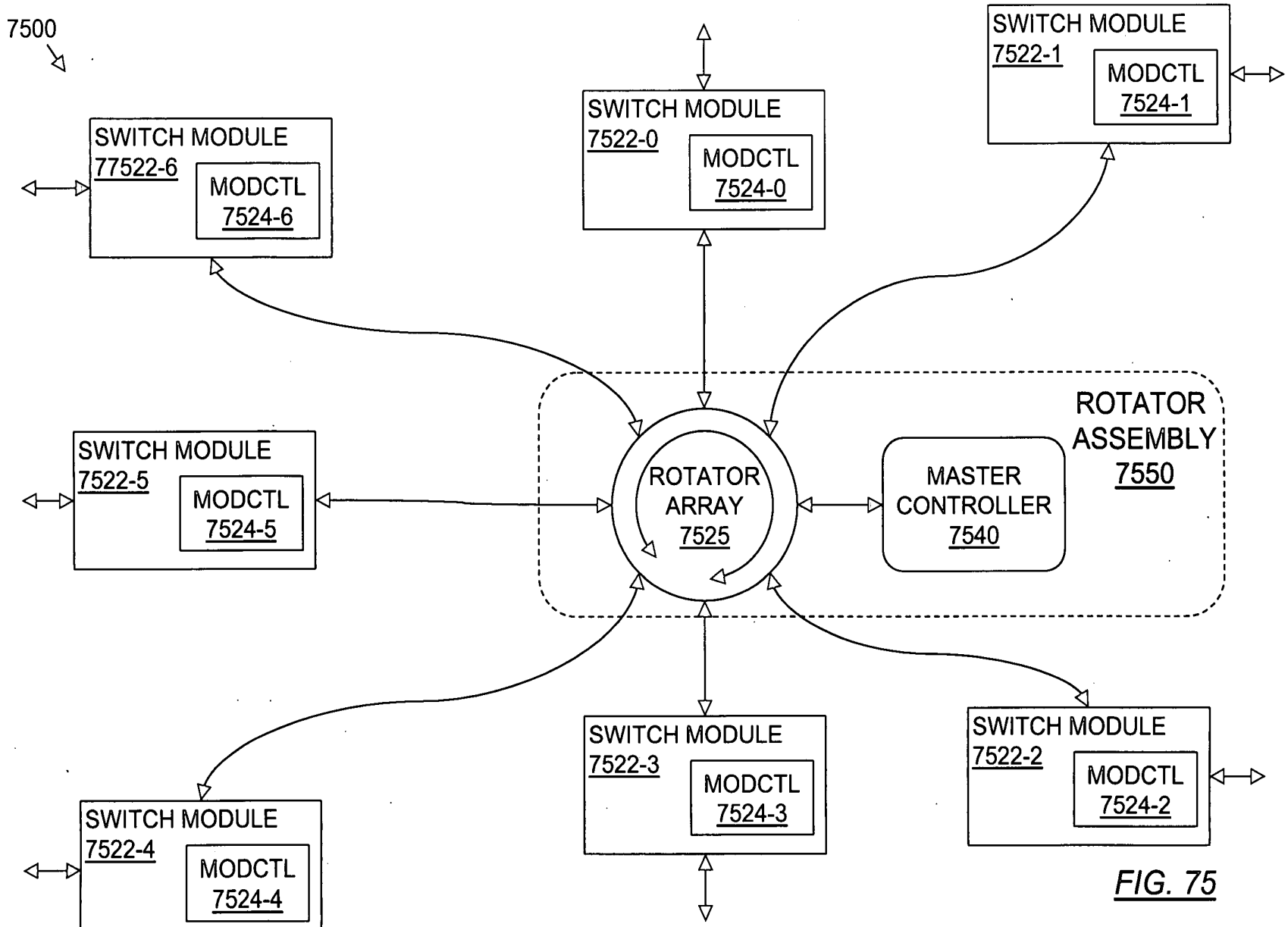

7500
SWITCH MODULE
77522-6
MODCTL
7524-6
SWITCH MODULE
7522-0
MODCTL
7524-0
SWITCH MODULE
7522-1
MODCTL
7524-1
SWITCH MODULE
7522-5
MODCTL
7524-5
ROTATOR
ARRAY
7525
MASTER
CONTROLLER
7540
ROTATOR
ASSEMBLY
7550
SWITCH MODULE
7522-4
MODCTL
7524-4
SWITCH MODULE
7522-3
MODCTL
7524-3
SWITCH MODULE
7522-2
MODCTL
7524-2

FIG. 75

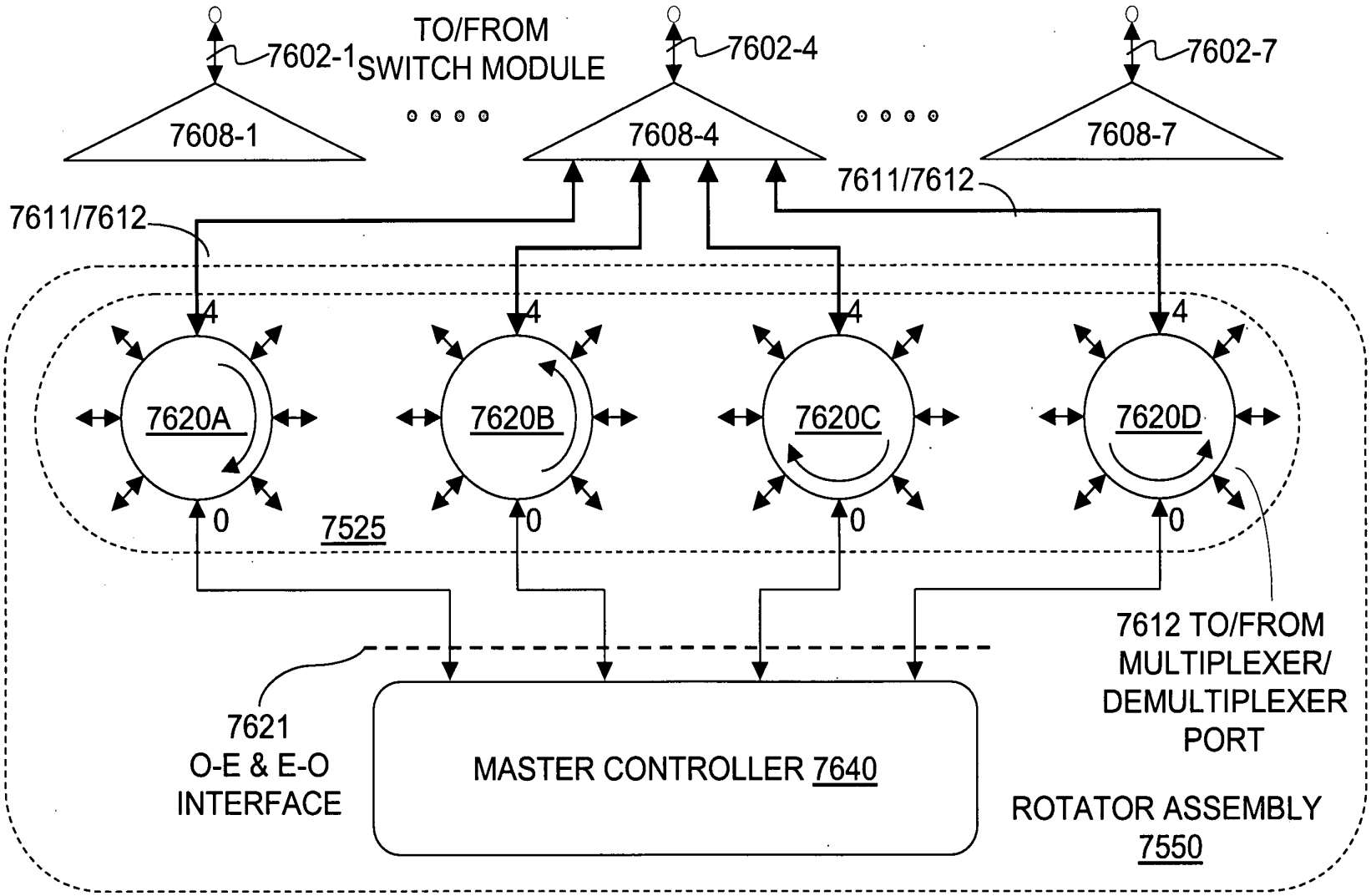

TO/FROM
SWITCH MODULE
7602-1
7602-4
7602-7
7608-1
7608-4
7608-7
7611/7612
7611/7612
4
4
4
4
7620A
7620B
7620C
7620D
0
0
0
0
7525
7612 TO/FROM
MULTIPLEXER/
DEMULTIPLEXER
PORT
7621
O-E & E-O
INTERFACE
MASTER CONTROLLER 7640
ROTATOR ASSEMBLY
7550

FIG. 76

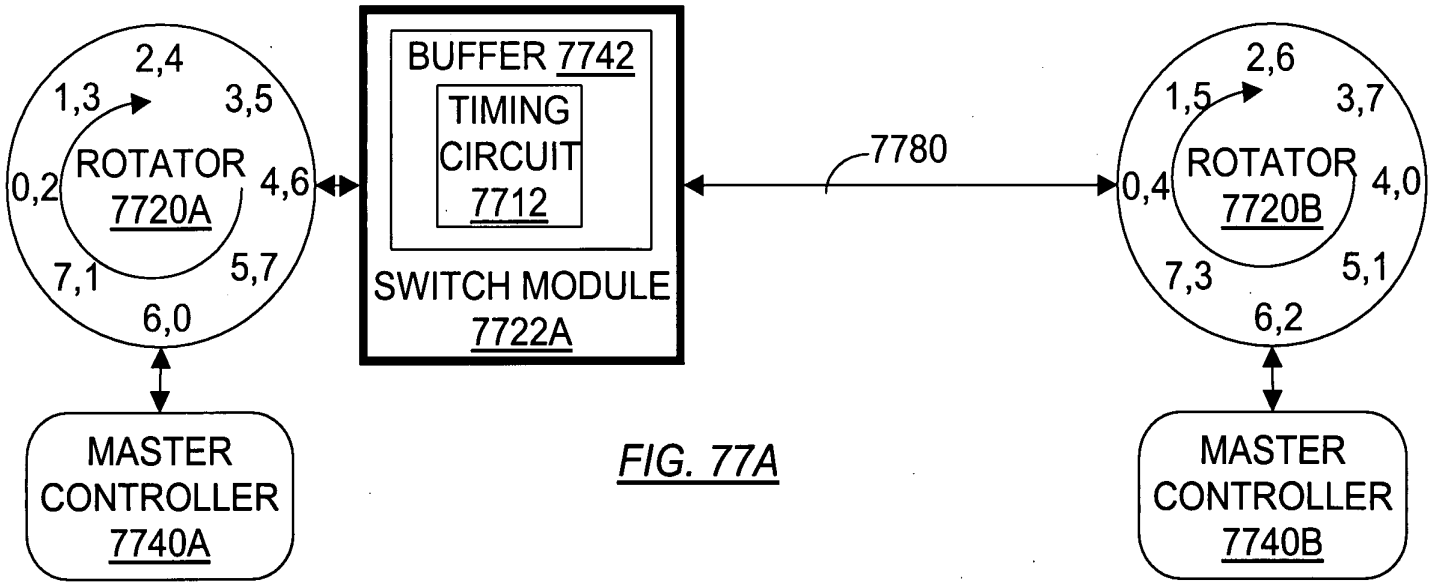


FIG. 77A

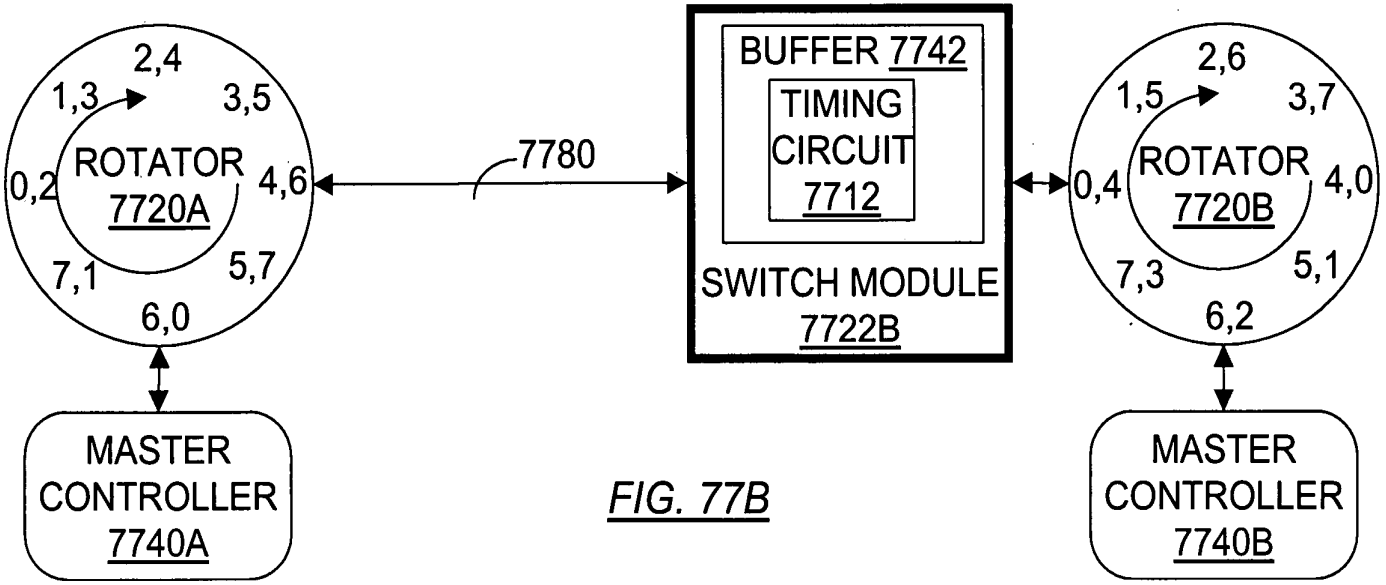


FIG. 77B

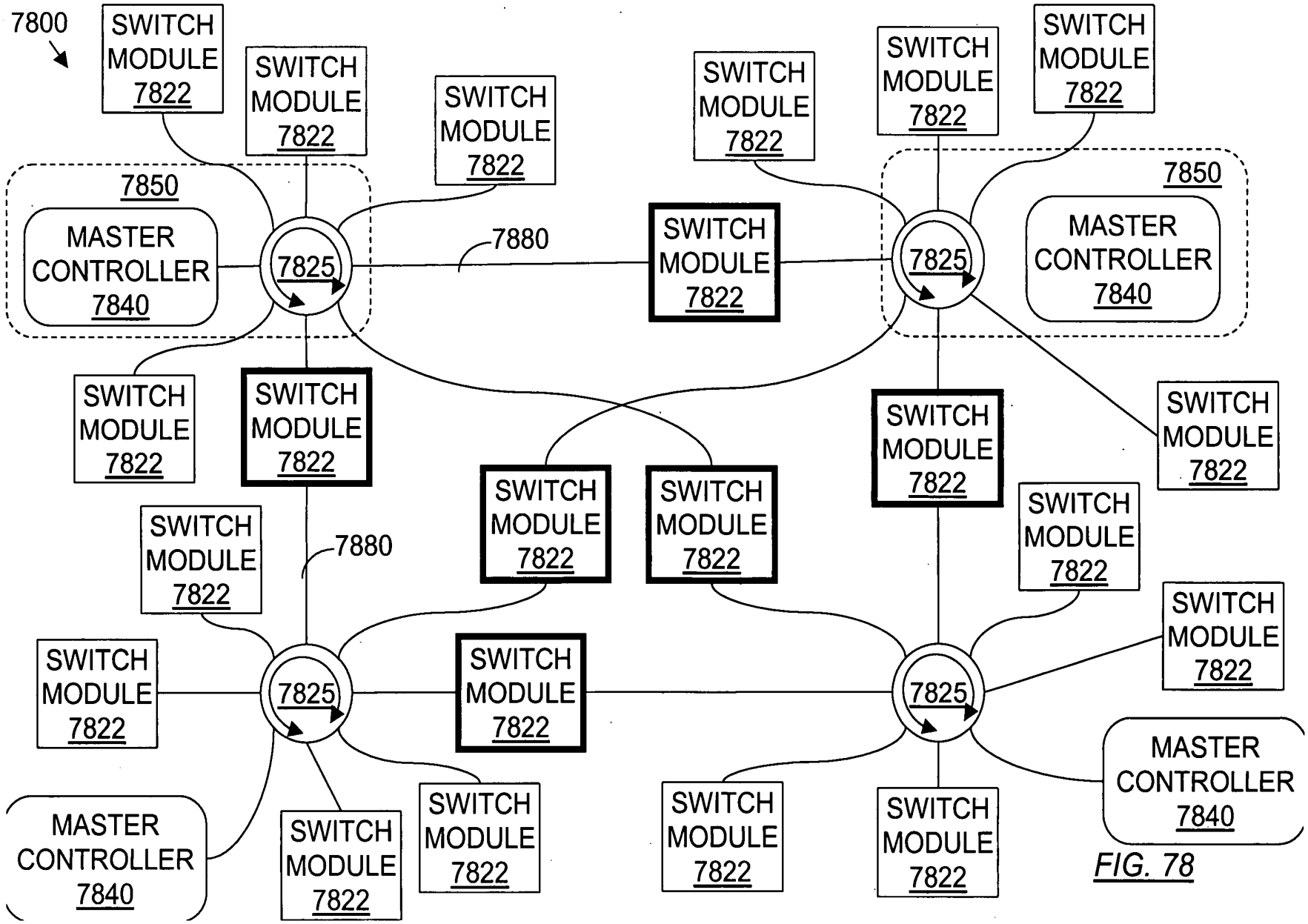

7800
SWITCH MODULE 7822
SWITCH MODULE 7822
SWITCH MODULE 7822
SWITCH MODULE 7822
SWITCH MODULE 7822
SWITCH MODULE 7822
7850
MASTER CONTROLLER 7840
7825
7880
SWITCH MODULE 7822
7825
7850
MASTER CONTROLLER 7840
SWITCH MODULE 7822
SWITCH MODULE 7822
SWITCH MODULE 7822
SWITCH MODULE 7822
SWITCH MODULE 7822
SWITCH MODULE 7822
7880
SWITCH MODULE 7822
SWITCH MODULE 7822
SWITCH MODULE 7822
SWITCH MODULE 7822
7825
SWITCH MODULE 7822
7825
SWITCH MODULE 7822
MASTER CONTROLLER 7840
SWITCH MODULE 7822
SWITCH MODULE 7822
SWITCH MODULE 7822
SWITCH MODULE 7822
MASTER CONTROLLER 7840

FIG. 78

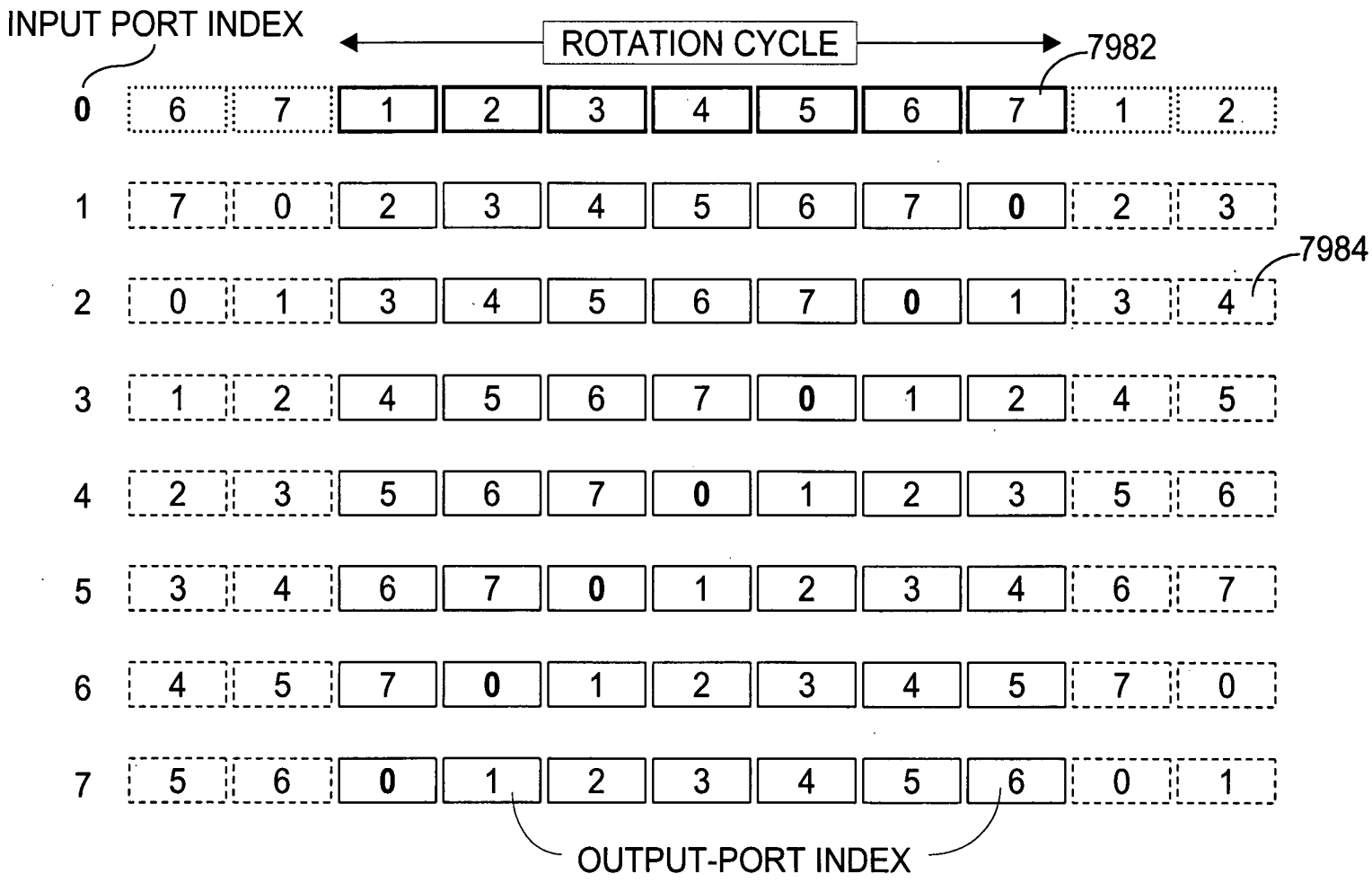

INPUT PORT INDEX
ROTATION CYCLE
7982
7984
0 6 7 1 2 3 4 5 6 7 1 2
1 7 0 2 3 4 5 6 7 0 2 3
2 0 1 3 4 5 6 7 0 1 3 4
3 1 2 4 5 6 7 0 1 2 4 5
4 2 3 5 6 7 0 1 2 3 5 6
5 3 4 6 7 0 1 2 3 4 6 7
6 4 5 7 0 1 2 3 4 5 7 0
7 5 6 0 1 2 3 4 5 6 0 1
OUTPUT-PORT INDEX

FIG. 79

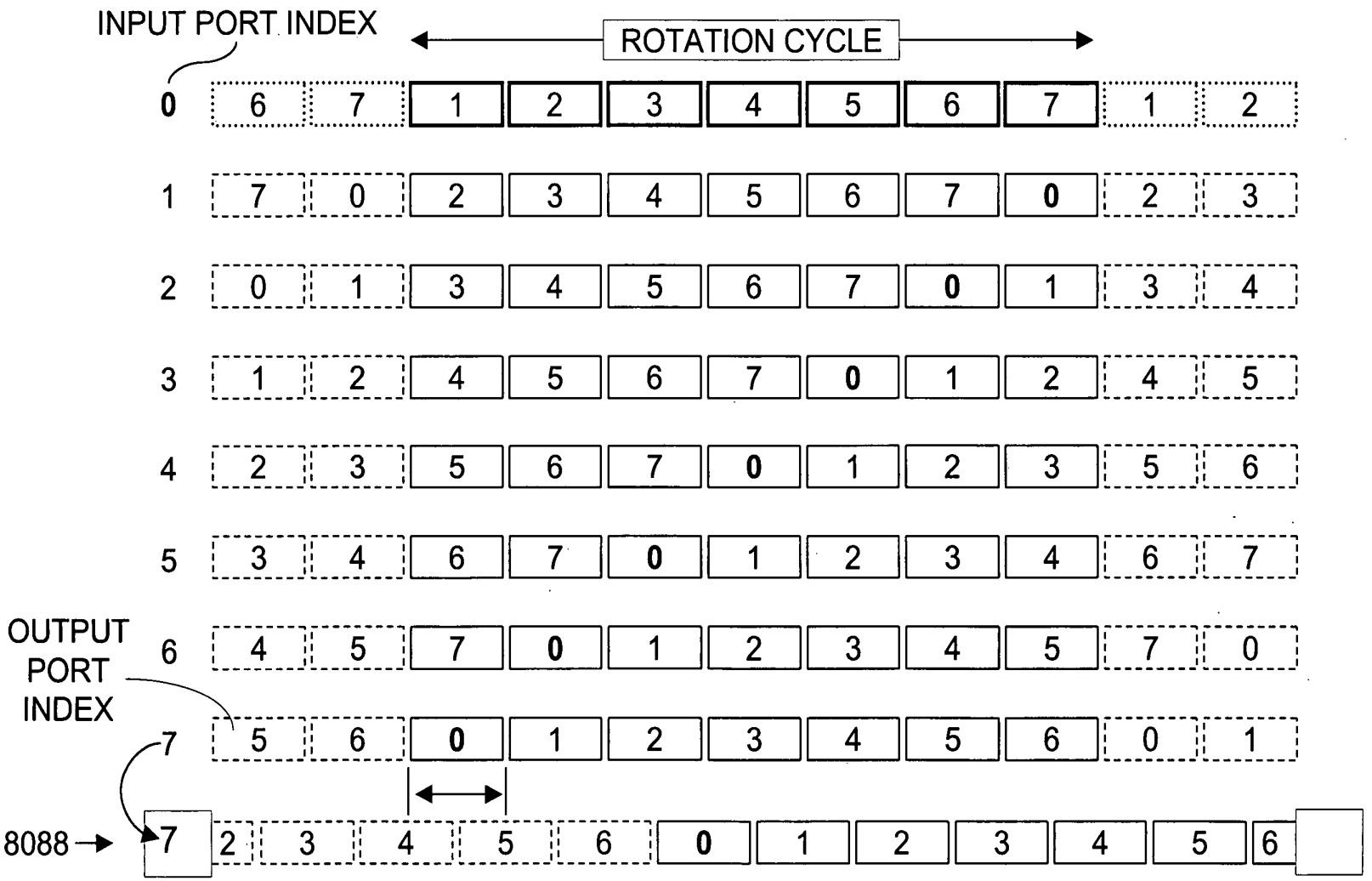

INPUT PORT INDEX
ROTATION CYCLE
0 6 7 1 2 3 4 5 6 7 1 2
1 7 0 2 3 4 5 6 7 0 2 3
2 0 1 3 4 5 6 7 0 1 3 4
3 1 2 4 5 6 7 0 1 2 4 5
4 2 3 5 6 7 0 1 2 3 5 6
5 3 4 6 7 0 1 2 3 4 6 7
OUTPUT PORT INDEX
6 4 5 7 0 1 2 3 4 5 7 0
7 5 6 0 1 2 3 4 5 6 0 1
8088
7 2 3 4 5 6 0 1 2 3 4 5 6

FIG. 80